A PFC Based Bridgeless Converter with Improved Power Quality for Welding Applications

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Abstract—**A Power Factor Corrected (PFC) two stage, Bridgeless (BL) Cuk converter based switched mode power supply is proposed in this work for arc welding applications. The absence of input Diode Bridge Rectifier (DBR) reduces the conduction losses and improves the thermal utilization of the converter's switches. The front-end comprises of a BL-Cuk converter operating in Discontinuous Conduction Mode (DCM) to attain unity Power Factor (PF) at the AC mains while at the back end, a PWM isolated Full Bridge (FB) DC-DC converter is used to regulate the output DC voltage. The performance of the system is examined in terms of the input PF, Total Harmonic Distortion (THD) of the ac mains current, voltage regulation and robustness. The obtained dynamic characteristics of this proposed topology depicts a constant voltage mode in various ranges of welding currents and inherent parametrical short circuit protection. Simulation results are presented to confirm the effectiveness of the proposed Arc Welding Power Supply (AWPS) in terms of excellent Power Quality (PQ).**

Keywords—**Arc Welding Power Supply (AWPS), Bridgeless, Power Quality, Total Harmonic Distortion (THD), Cuk Converter.**

I. INTRODUCTION

Modern Arc Welding Power Supply (AWPS) employs controllable high frequency (HF) DC-DC power converter(s) with excellent dynamic and steady state performance compounded with stringent voltage-current regulation. Generally, robustness, portability and simplicity are amongst the prevailing design criteria [1] for the AWPS. Moreover, to ensure suitably systematized metal droplet transfer through the established arc, AWPS should limit the welding load current even during the short circuit condition and must operate satisfactorily over a very wide load range i.e. from rated load to short-circuit condition. Also, a broad span of controlled load current is essential to enhance the welding action. Thus, in order to control the welding characteristics, the output DC voltage along with the output DC current, must always be regulated [2].

Mainly the conventional switched mode power supplies (SMPSs) for welding applications comprise a front-end uncontrolled diode bridge rectifier (DBR) followed by a bulk DC-link capacitor [3]. The presence of the DBR generally leads to problems such as high conduction loss and increased harmonic currents thus creating interference in power and communication lines. In the past few years, bridgeless (BL) power factor corrected (PFC) converters have gained huge attention and popularity due to their higher efficiency. In an effort to improve the Power Quality (PQ) of the SMPSs, various BL boost converter based topologies have been reported in the literature [4] adhering to the stringent requirements put forth by the international PQ standard IEC 61000-3-2 [5].

A considerable amount of work on BL boost PFC converter has been carried out because of its low cost, simplicity and high performance in terms of efficiency and PF. Nonetheless, the BL boost PFC converter suffers from some major limitations such as high start-up inrush current, lack of current limiting during overload conditions and ineptness to step down the input voltage. However, these are some of the essential prerequisites in designing an SMPS for welding applications. A BL buck converter has a poor PFC capability and also does not support short-circuit operating conditions. Among various buck-boost converters, Cuk converter offers high quality input and output currents due to the presence of inductors at both input and output side of the converter [6]. Thus, considering a BL PFC Cuk converter that is capable of yielding lower voltage at the output would be a viable alternative.

The objective of this paper is to design and model a single phase AWPS using BL-Cuk converter at the front end and a PWM full-bridge (FB) DC-DC converter for high-frequency isolation at the load end. Its meritorious features include output voltage stability and short-circuit withstand capability. The BL-Cuk converter is designed to operate in Discontinuous Conduction Mode (DCM) to attain inherent PFC at the input AC mains [7-8]. Independent closed loop control functions are used in both stages. A Pulse Width Modulation (PWM) control strategy has been implemented with a constant switching frequency of 50 kHz. Its fast dynamic response during load variations leads to a better arc stability and uniform weld bead quality. The detailed analysis and design of the proposed AWPS are discussed in following sections to illustrate its improved performance in terms of unity PF and reduced THD in the AC mains current at different loads and supply voltage conditions. The efficacy of the proposed improved PQ AWPS is demonstrated by means of simulation results using MATLAB/SIMULINK tool.

II. PROPOSED BL CONVERTER BASED AWPS

The proposed BL-Cuk converter based AWPS is shown in Fig. 1. The absence of front end DBR and the presence of only two semiconductor switches (one diode and one power switch) in the current flowing path during each switching cycle minimizes the conduction losses and improves the thermal management as compared to the conventional PFC converters. In this topology, two Cuk DC-DC converters are connected back-to-back followed by an isolated FB buck converter.

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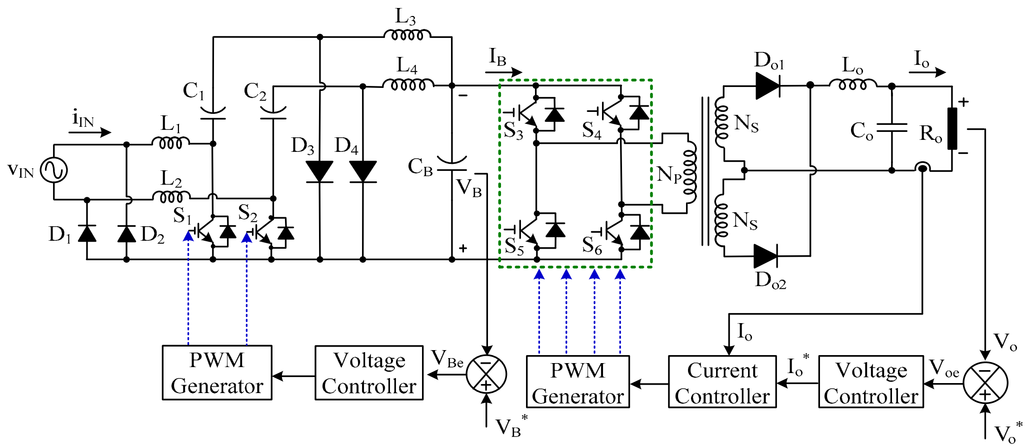


Fig.1. Schematic of BL Cuk converter and isolated FB converter based AWPS.

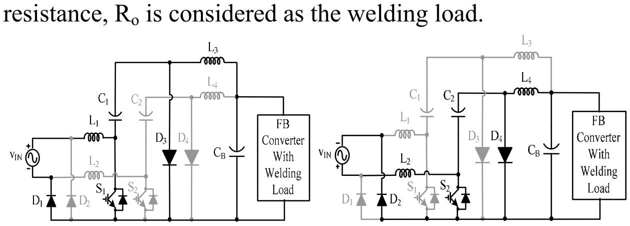
Fig. 2a and 2b depict the operation of the proposed topology during positive and negative half cycles of the input ac mains. Out of the two back-to-back connected Cuk converters, one operates during the positive half and the other during the negative half of the power frequency cycle. This further brings down the thermal stresses, as well as conduction losses.

A. Configuration

The proposed circuit (Fig.1) comprises of a single phase AC mains feeding two Cuk converters which, in turn, feed a FB buck converter having a high frequency transformer (HFT) and a welding load.

The first stage consisting of the PFC BL-Cuk converter rectifies the input AC mains voltage into an intermediate regulated DC voltage. The second stage is formed by using an isolated FB buck converter, to convert the output of the BL-Cuk converter into a DC output voltage of desired magnitude. The DCM operation of the output inductors (L_3 and L_4) of BL-Cuk converter results in an excellent PF pre-regulator operation and adds additional features such as zero current turn-on in the power switches S_1 and S_2, and zero-current turn-off in diodes D_3 and D_4. This in turn, minimizes the turn-on switching losses of the power switches and enhances the reverse recovery of the output diodes significantly.

In the second stage, the FB buck DC-DC converter comprises of four power switches (S_3, S_4, S_5 and S_6), a HFT with its secondary center-tapped, a half-wave rectifier and an L_o-C_o filter at the output side. Since work-piece is a part of the power supply circuit, it must be earthed; thus, an isolation transformer is essential in AWPS to ensure safety. The resistance, R_o is considered as the welding load.



(a) (b)

Fig.2. Operating circuits of the proposed BL Cuk converter based AWPS during positive and negative half-cycles of the supply voltage.
(a) during positive half cycle; (b) during negative half cycle.

B. Operating Stages

The proposed BL AWPS is formed by connecting two Cuk converters, each functioning over a half-cycle period of the supply voltage. The operating principle of the BL-Cuk converter is explained for one half cycle of the supply frequency; in the other half cycle also the converter performs in a similar manner.

As shown in Fig. 2(a), during the positive half-cycle, switch S_1, inductors L_1 and L_3, diodes D_1 and D_3 and capacitors C_1 transfer the energy from the source to the DC-link capacitor, C_B. The voltage V_B across the DC-link capacitor C_B is controlled and fed as an input to the isolated FB converter. Likewise, L_2-S_2-C_2-L_4-D_4, conduct through diode D_2 during the negative half cycle of the input voltage as shown in Fig. 2(b). For the analysis, all semiconductor devices are assumed to be ideal. The capacitances C_B and C_o are sufficiently large such that the voltage ripple across them can be neglected. The inductors L_3 and L_4 are designed such that the current through these inductors become discontinuous during each switching cycle. For the positive half-cycle of the input voltage, v_{in}, there are three intermediate operating stages of the BL-Cuk converter for every switching cycle which are described as follows.

Stage I: Referring to Fig. 3(a), when power switch S_1 is turned on, a positive supply voltage, v_{in} is applied to the input inductor, L_1. So, the current through the input inductor, i_{L1} starts increasing linearly and flows through diode D_1. The intermediate capacitor C_1 is discharged through the output inductor, L_3 and the DC-link capacitor, C_B thereby energizing the inductor, L_3. Hence the current, i_{L3} also rises linearly.

Stage II: During the turn-off state of S_1, diode D_3 becomes forward biased providing a path for the inductor currents, i_{L1} and i_{L3}. The inductors, L_1 and L_3 transfer the stored energy to the capacitors C_1 and C_B respectively. Thus the inductor currents start falling linearly. This interval continues till the inductor currents become equal and opposite (i.e. i_{L1}= -i_{L3}) and current through the diode, D_3 reaches zero.

Stage III: This stage is initiated when both switch S_1 and the diode D_3 are turned off as the sum of inductor currents i_{L1} and i_{L3} becomes zero. Thus the converter enters into DCM operation as shown in Fig. 3(c). The currents through inductors L_1 and L_3 remain constant and continue to charge the intermediate capacitor, C_1. Consequently, the DC-link capacitor C_B discharges to supply the load i.e. FB converter connected to it. The inductors act as current sources and the voltages across them is zero throughout this interval. Fig. 3(d) illustrates the DCM waveforms during the positive half cycle of the supply voltage over one PWM switching period. Stage III is completed when switch S_1 is triggered to restart the operating cycle again.

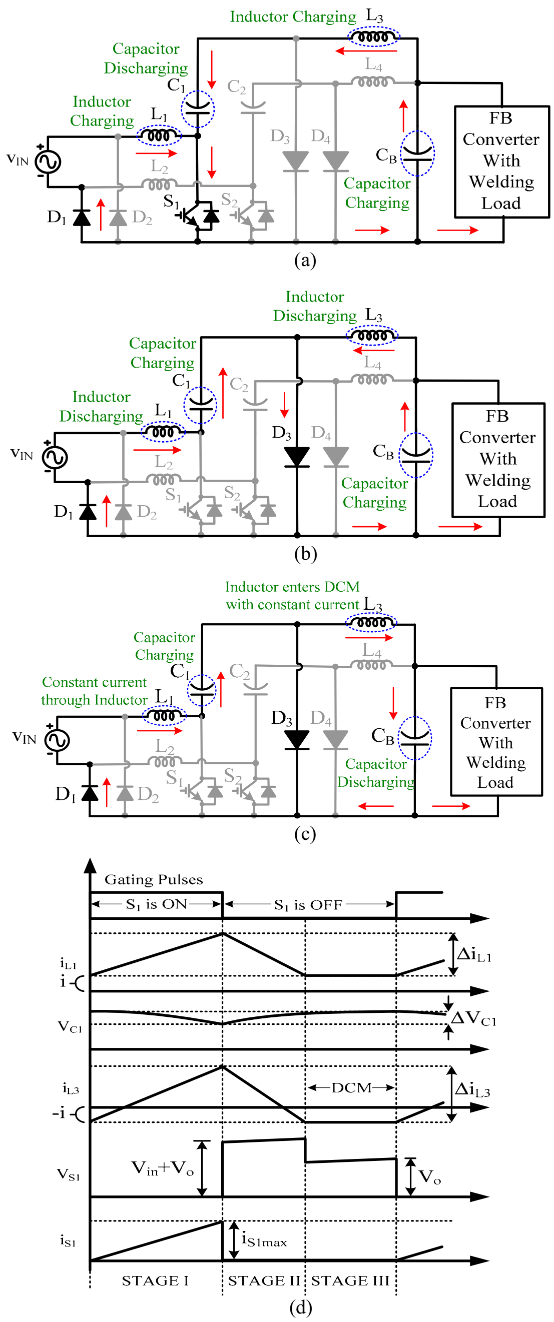


Fig.3. Operating stages of BL Cuk converter during steady state. (a) Stage I; (b) Stage II; (c) Stage III; (d) Waveforms during one switching period.

The controlled DC output (V_B, I_B) of the BL-Cuk converter is further fed to the FB buck converter which is intended to operate in Continuous Conduction Mode (CCM). In the FB converter, the switching pairs S_3-S_6 and S_4-S_5 are turned on alternately during each half cycle of a switching period. The voltage V_B, is applied across the primary winding of the HFT. When both the switching pairs are turned off, then the output rectifier diodes D_{o1} and D_{o2} act as freewheeling diodes. At the output, L_o-C_o filter provides a ripple-free output DC voltage.

C. Control Strategy

Pulse Width Modulation (PWM) technique is used with a constant switching frequency (=50kHz) to ensure DCM operation of the BL-Cuk converter. This minimizes the number of sensors required thereby cutting down on the cost. However, the same control signal can be used to drive both power switches, S_1 and S_2, which considerably simplifies the control circuit. With minimal amount of control circuitry, the proposed AWPS design is very compact and economical. The BL converters are operated in DCM by incorporating voltage mode control technique. The DCM operation of the PFC stage ensures high PF at the input and excellent voltage regulation at the output DC-link. The DC-link voltage, V_B is compared with the reference voltage, V_B^* to generate the voltage error, V_{Be} which is fed to a Proportional-Integral (PI) controller whose output is compared with a 50 kHz ramp signal to generate the firing signals for the switches S_1 and S_2. The PI controller provides excellent line-load regulation.

Dual loop control scheme is employed in the isolated FB converter to incorporate short circuit protection. The sensed output DC voltage, V_o is compared with the reference DC voltage, V_o^*. This error voltage signal, V_{oe} is further fed to another PI voltage controller to generate a reference signal, I_o^*. This serves as the reference for the output load current, I_o. Now, I_o^* is compared with the actual I_o so that it is prevented from exceeding the desired limit. The output of the PI current controller is given to the PWM generator where it is compared with the HF ramp signal to generate gating pulses for the isolated FB converter.

III. Design of Proposed BL Converter Based AWPS

The complete design and analysis of the BL converter based AWPS are presented in this section. During the analysis, the power switches and the diodes are assumed to be ideal. In order to derive the necessary component design, the supply voltage, v_{in} is considered to be a constant during one switching frequency (f_s) cycle as f_s is much higher than the line frequency, f.

A. Design of BL-Cuk Converter

For the sake of simplicity, a single module of Cuk converter, operating in positive half cycle of the supply voltage is considered for this analysis. The PFC BL-Cuk converter is designed to maintain a constant DC-link voltage (V_B) of 400 V with the inductors (L_3 and L_4) operating in DCM. The average value, V_{inav} of the supply voltage ($v_{in,rms}$ = 220 V) is given as,

$$V_{inav} = \frac{2\sqrt{2}v_{in}}{\pi} = \frac{2\sqrt{2}*220}{\pi} = 198.07\text{V} \tag{1}$$

On applying the volt-second balance to the BL Cuk converter, one obtains,

$$\frac{V_B}{V_m} = \frac{D_B}{\sqrt{K}}; \qquad (2)$$

$$\text{where, } K = \frac{2f_s}{R_B}\left(\frac{L_1L_3}{L_1+L_3}\right) = \frac{2f_sL_{eq}}{R_B}; \qquad (3)$$

$$L_{eq} = \frac{L_1L_3}{L_1+L_3}; \qquad (4)$$

$$R_B = \frac{V_B}{I_B} = \frac{400}{5} = 80\,\Omega\,; \qquad (5)$$

Also, D_B is the on-time of the power switches S_1 and S_2, V_B is the DC-link voltage and f_S is the switching frequency (=50kHz) of the BL Cuk converter.

The integral of the inductor voltages must be zero over one switching period. Thus the expression for duty cycle, D_B is given by,

$$D_B = \frac{V_B}{V_{inav}+V_B} = \frac{400}{198.07+400} = 0.668 \qquad (6)$$

In order to operate the converter in DCM,

$$K < K_c < \frac{{V_m}^2}{2(V_m+V_B)^2} < \frac{(311)^2}{2(311+400)^2} < 0.0956 \qquad (7)$$

The value of K is taken around two-thirds of K_c to ensure DCM operation of the proposed BL Cuk converter.

Thus, K is selected as 0.06373.

$$L_{eq} = \frac{R_BK}{2f_s} = \frac{80*0.06373}{2*50000} = 50.984\ \mu H \qquad (8)$$

If Δi_{L1} and Δi_{L3} are considered to be the permissible current ripple in the inductors L_1 and L_3 respectively, then the change in inductor currents (Δi_{L1} and Δi_{L3}) is determined from the on period of the semiconductor devices as,

$$\Delta i_{L1} = \frac{V_{inav}D_B}{L_1f_s};$$

$$\text{thus, } L_1 = \frac{D_BV_{inav}}{f_s(\Delta i_{L1})} = \frac{0.668*198.07}{50000*1.993} = 1.327\text{ mH} \qquad (9)$$

where f_S is 50 kHz. The value of the input inductor, L_1 is estimated to be 1.5mH.

Using eqns. (4), (8) and (9),

$$L_3 = \frac{L_1L_{eq}}{L_1\text{-}L_{eq}} = \frac{(1.327*10^{-3})(50.984*10^{-6})}{(1.327*10^{-3})-(50.984*10^{-6})} = 53.021\mu H \qquad (10)$$

The selected value of inductor, L_3 is 40 μH to achieve DCM operation. To minimize the input current oscillation, the resonant frequency of C_1, L_1 and L_3 should be greater than the line frequency. Moreover, the resonant frequency of C_1 and L_3 must be less than the switching frequency to attain constant voltage during every switching cycle. Therefore, the value of the intermediate capacitor, C_1 can be approximated as,

$$C_1 = \frac{1}{{\omega_r}^2(L_1+L_3)} \qquad (11)$$

$$= \frac{1}{(2\pi*5000)^2(1.327*10^{-3}+53.021*10^{-6})} = 0.734\ \mu F$$

where $\omega_L < \omega_r < \omega_s$; ω_L = line frequency, ω_r = resonant frequency, ω_s = switching frequency

The resonant frequency is selected to be 5 kHz.

The DC-link capacitor, C_B value can be calculated from eqn. (8) for a given voltage ripple in the DC-link voltage, V_B as,

$$C_B = \frac{I_B}{4\pi f(\Delta V_B)} = \frac{5}{4*\pi*50*40} \cong 0.2\text{ mF} \qquad (12)$$

B. Design of Isolated FB Buck Converter

For an isolated FB buck converter operating in CCM, the voltage conversion ratio can be derived by applying the constant volt-second relationship on the output inductor, L_o.

$$\left\{V_B\left(\frac{N_S}{N_P}\right)-V_o\right\}\left(\frac{t_{on}}{T_s}\right)-\left\{V_o\left(\frac{t_{off}}{T_s}\right)\right\}=0 \qquad (13)$$

Thus the duty cycle, D_f for switches S_1, S_2, S_3, S_4, is given as,

$$D_f = \frac{V_o}{2V_B}\left(\frac{N_P}{N_S}\right) \qquad (14)$$

$$\text{Considering } D_f = 0.35,\ \left(\frac{N_P}{N_S}\right) = \frac{0.35*2*400}{20} = 14.$$

If the permissible ripple current is Δi_{Lo} (10% of I_o) then the value of output inductor, L_o for CCM operation can be estimated as,

$$L_o = \frac{V_o(0.5-D_f)}{f_s(\Delta i_{Lo})} = \frac{20*(0.5\text{-}0.35)}{50000*10} = 6\mu H \qquad (15)$$

To ensure CCM operation of the inductor, the selected value of L_o= 9μH.

The voltage ripple on output capacitor C_o is calculated as,

$$\Delta V_o = \frac{V_o(1-2D_f)}{32\,{f_s}^2L_oC_o} \qquad (16)$$

The output capacitor value is calculated for a given voltage ripple as,

$$C_o = \frac{V_o(1-2D_f)}{32{f_s}^2L_o(\Delta V_o)} = \frac{20*(1\text{-}0.7)}{32*50000^2*6*10^{-6}*2} \cong 7\mu F \qquad (17)$$

The complete design specifications for both the converters (BL Cuk and isolated FB buck converter) calculated using the above equations are listed in the Appendix.

IV. Performance Evaluation of the Proposed BL Converter Based AWPS

In order to validate the design and operation of the proposed converter, it is modeled in MATLAB/ SIMULINK environment. The performance of the proposed BL converter based AWPS is analyzed on the basis of several performance indices. The waveforms presented are AC mains voltage (v_{in}), source current (i_{in}), DC-link voltage (V_B), DC-link current (I_B), output DC arc voltage (V_o), output welding load current (I_o), switch stress (V_s, I_s), inductor currents (i_{L1}, i_{L3}) and intermediate capacitor voltage (V_{C1}). The effects of supply voltage and load variations on various PQ indices such as PF, Displacement Power Factor (DPF), Distortion Factor (DF) and THD are examined to demonstrate the improved PQ operation of the proposed power supply.

The steady state behavior of the proposed AWPS at rated load condition is presented in Fig. 4. It clearly depicts that during the positive half cycle, S_1 conducts while S_2 is active during the negative half cycle of the supply voltage. The inductor current, i_{L3} waveform confirms the DCM operation of the BL-Cuk converter. Apart from the steady state performance, the converter response with closed loop control is demonstrated in Fig. 5 with a load step change of 100% to 20% of the rated load and vice versa is applied on the SMPS. It can be clearly seen that when the welding load current is suddenly decreased from 100A to 20A, the PI controller maintains a constant DC voltage. The input current waveform and harmonic spectrum at rated load and light load are presented in Fig. 6(a) and (b) respectively, indicating that the THD is well within the acceptable limits and the input current is sinusoidal attaining unity PF.

In Figs. 7 and 8, the dynamic performance of the proposed AWPS on varying the supply voltage is demonstrated. When the voltage is changed from 220 V (rms) to 170 V and 270 V, it is seen that the proposed system responds quickly confirming fast dynamic response and optimized PI controller.

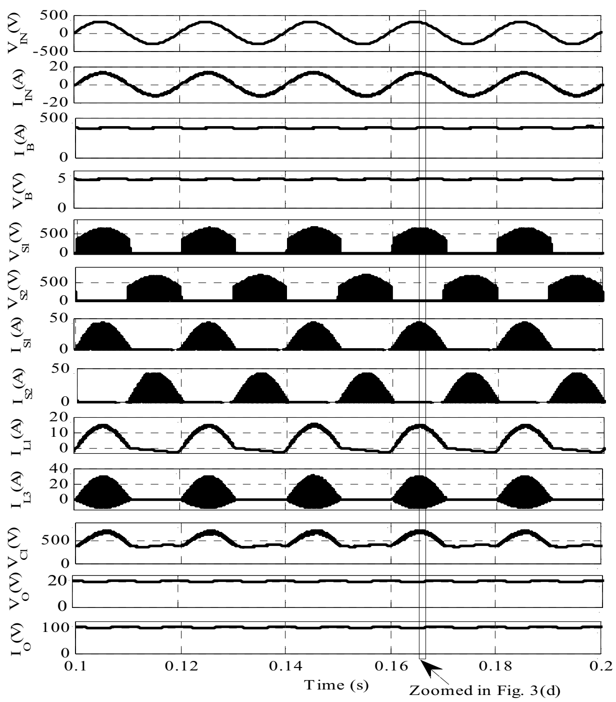


Fig.4. Steady state behavior of proposed AWPS at 220 V AC mains and 100% load.

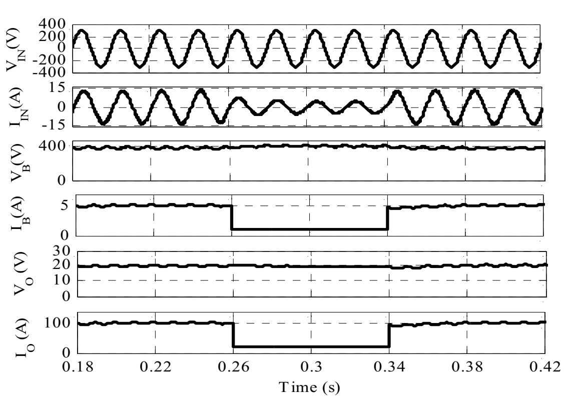
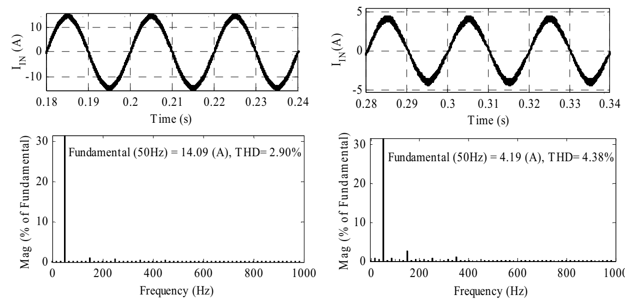


Fig.5. Dynamic performance of the proposed AWPS at 20% load.



(a) (b)

Fig. 6. Harmonic spectra of AC mains current, I_{IN}
(a) at 220 V AC mains and 100% load; (b) at light load conditions

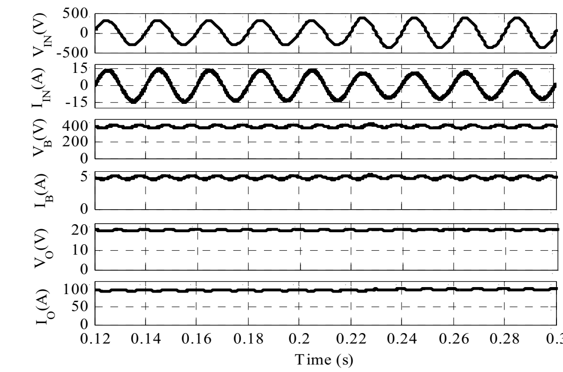


Fig.7. Dynamic performance of the proposed AWPS at V_{IN} of 170 V and full load condition.

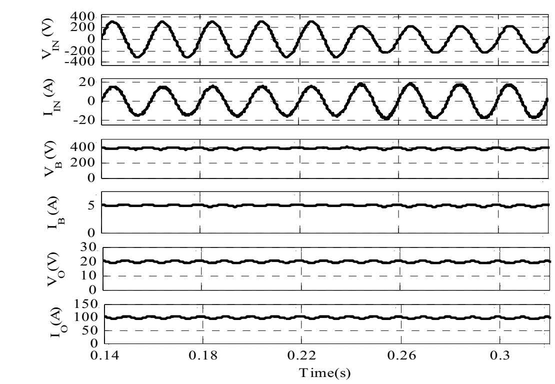
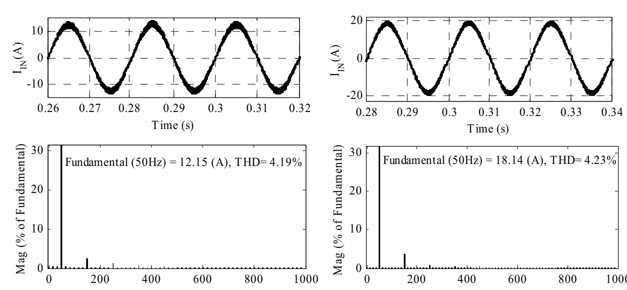


Fig.8. Dynamic performance of the proposed AWPS at V_{IN} of 270 V and full load condition.



(a) (b)

Fig.9. Harmonic spectra of AC mains current, I_{IN}
(a) at 270 V AC mains and full load; (b) at 170 V AC mains and full load.

Figs. 9(a) and 9(b) show the input current waveform along with the harmonic spectra at 170V and 270V respectively. It can be observed that the input AC mains current is in phase with the input voltage maintaining the THD below 5%.

While designing an AWPS, fast dynamic response and short circuit protection are amongst the indispensable features. Accordingly, it is beneficial to have a short circuit current a bit higher than the normal load current to inhibit the electrode from sticking to the work-piece during the arc striking process. The short circuit also occurs when the electrode accidentally comes in contact with the welding pad and gets glued with the molten metal.

The short circuit withstand capability of DC AWPS is illustrated in Fig. 10. The dual-loop controller limits the current to 125 A which will consequently improve the weld bead quality. The impact of load as well as supply voltage variations on various PQ indices such as PF, DPF and DF are shown in Figs. 11-12 respectively. It is evident from these waveforms that the PF is approaching unity and THD is always less than 5% which is within the limits specified by IEC 61000-3-2 standards.

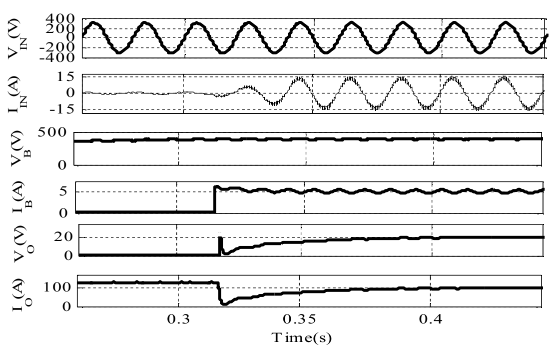
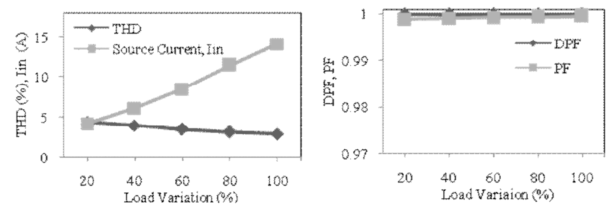


Fig.10.Dynamic performance of the proposed AWPS during over-current condition (i.e. transition from short-circuit to full load).

V. CONCLUSION

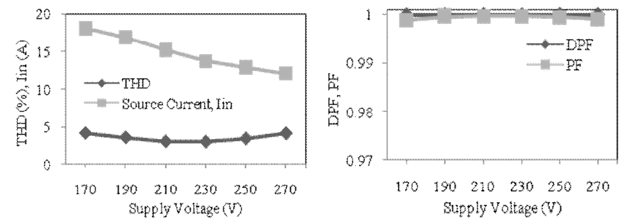
A BL-Cuk converter based 2 kW AWPS has been designed with low input current THD and less conduction losses. The proposed circuit topology is a good solution as it offers excellent PFC features at the front end while the FB converter provides output isolation along with the over-current and start-up protection. The component count has also reduced by integrating two power conversion stages. The quality of weld is enhanced by controlling the output side parameters to regulate the heat and mass input to the weld pool.

Furthermore, it can be inferred from the obtained results that the proposed BL converter based system has provided robustness and fast response. It is evident from the obtained results that the THD of the AC mains current is well below 5% for both full load as well as light load conditions and for the complete range of operating AC mains voltage from 170V to 270V. The PF has also remained close to unity making it suitable for wide-range of line/load operations. In all, it can be concluded that the proposed BL converter based topology conforms to the requirements of the international standard IEC 61000-3-2 expected out of an AWPS.



(a) (b)

Fig.11. PQ indices of proposed AWPS under different load conditions.
(a) Source current, I_{IN} and its THD at various load conditions
(b) DPF and PF at various load conditions



(a) (b)

Fig.12. PQ indices of proposed AWPS under various supply voltage conditions. (a) Source current, I_{IN} and its THD at different supply voltage conditions; (b) DPF and PF at different supply voltage conditions

APPENDIX

Specifications of Proposed AWPS

Input single phase supply voltage, V_{in}(rms): 220 V, 50Hz; Output Power, P_o: 2.0kW; Output Arc Voltage, V_o: 20V; Output Welding Current, I_o: 100A; Switching Frequency of BL Cuk Converter: 50kHz; BL Cuk Input Inductors (L_1, L_2): 1.5mH; BL Cuk Output Inductors (L_3, L_4): 53.021μH; Intermediate Capacitors (C_1, C_2): 0.734μF; DC-Link Capacitor (C_B): 0.2 mF; Switching Frequency of Isolated FB Converter: 50kHz; HFT Turns Ratio (N_P/N_S): 14; Output Inductance (L_o): 9μH; Output Capacitance (C_o): 7μF.

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