A novel technique to achieve high bandwidth at low supply voltage

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***Abstract*—In this work we have demonstrated a novel technique to achieve high bandwidth in differential amplifier. This technique is based on using a composite transistor configuration consisting of dynamic threshold MOS transistor (DTMOS) and a source follower. This composite transistor has higher value of transconductance and bandwidth than conventional DTMOS. The use of this technique increases the bandwidth of differential amplifier by a factor of 3.36 at unity gain. Analytical and simulated results are in good agreement. All the circuits have been designed in 180nm CMOS technology. The proposed differential amplifier would find interesting applications for low voltage RF design.**

***Keywords*—Dynamic Threshold MOS transistor, high bandwidth, Low voltage, transconductance, source follower**

I. INTRODUCTION

There has been a continual increase in portable devices in various fields. As the advancement in technology is increasing and day to day life is becoming faster, demand for high speed and high bandwidth devices is rising[1,2]. High bandwidth requirement is inevitable in the field of telecommunications, telemedicine, multi point video conferencing etc. With the technology scaling, low-power and low-voltage analog and mixed mode circuits are gaining importance. The continuous trend toward smaller feature size for transistors in the CMOS technology demands for lower supply voltages. But the value of the threshold voltage (V_{th}) of MOS transistor doesn't proportionally decrease with device size reduction, which poses a great challenge to CMOS analog circuit design. This trend has forced most analogue basic building blocks to be redesigned, in an attempt to guarantee their overall same performance or better than their operation for larger power supplies. Many non conventional low voltage analog techniques have been reported [3].

Low voltage operation generally deteriorates the bandwidth of the circuit. One of the most promising ways to attain both high bandwidth and low stand-by power consumption at low supply voltage is to lower the threshold voltage of MOS transistor. Assaderaghi et al.in 1994 proposed a novel technique known as DTMOS [4]. In DTMOS technique body is connected directly to gate electrode of the MOS transistor as shown in Fig.1. Since the gate and body terminal are tied together, this results in forward bias of the body terminal and hence less number of charge carries will be present at the inversion layer so less amount of gate voltage will be required to balance the charge carriers in the inversion layer which will result in decrease of the threshold voltage. There is an increasing interest in the suitability of DTMOS for analog applications [5-7].

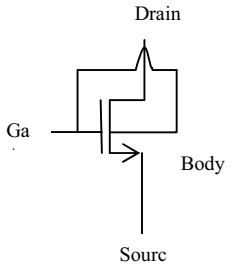

Fig. 1 Conventional DTMOS transistor

The source-body junction gets slightly forward biased when gate input increases. Owing to this effect the threshold voltage(V_{th}) decreases in the ON state of the transistor and increases in the OFF state. The Threshold voltage is given by following equation

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\emptyset_F| + V_{SB}} - \sqrt{|2\emptyset_F|}\right) \quad (1)$$

Where, V_{th} is threshold voltage when V_{SB} is not zero, V_{th0} is the threshold voltage at zero body bias and mainly depends on the manufacturing process. γ is the body effect factor/coefficient (typically equals to 0.4 $V^{0.5}$) and it depends on the gate oxide capacitance, silicon permittivity, doping level and other parameters. Φ_F is the surface potential at threshold (typically $|-2\varphi_F|$ equals 0.6 V). V_{SB} is the source-to-body voltage [6].

DTMOS technique requires the use of a triple well technology so that PMOS and NMOS bodies can be independently biased. This technique is fully compatible with existing CMOS designs and available tools thus can be applied in a very straightforward manner. At low drain current, DTMOS shows significantly higher cutoff frequency (f_t) and maximum frequency oscillator (f_{max}) performance[7,8].

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In this paper we have proposed to use source follower along with DTMOS transistor to increase the bandwidth of a differential amplifier. Rest of the paper is organized as as follows. In section 2 small signal analysis of composite transistor consisting of DTMOS and source follower is presented. In section 3, circuit implementation of proposed differential amplifier is given. Simulation results are provided in section 4 and finally Conclusions are summarized in section 5.

II. COMPOSITE TRANSISTOR CONFIGURATION

Fig.2 shows small signal model of conventional DTMOS transistor[9].

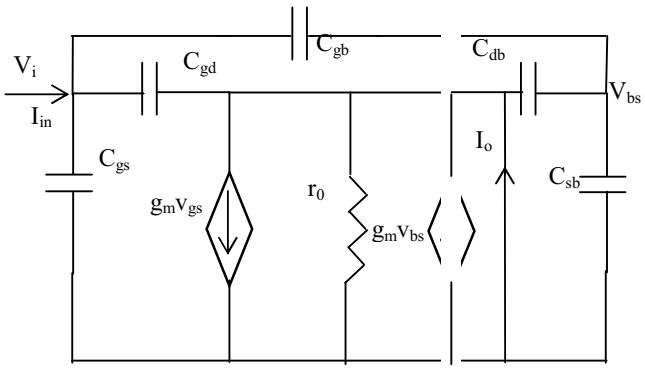

Fig. 2. Small signal model of conventional DTMOS

Analysis of Fig.2 gives following expressions

$$I_0 = V_i(g_m - sC_{gd}) + V_i \frac{C_{gb}}{(C_{sb}+C_{db}+C_{gb})}(g_{mb} - sC_{db}) \quad (2)$$

$$I_i = V_i s\left(C_{gd} + C_{gs} + C_{gb}\right) - V_i \frac{C_{gb}}{(C_{sb}+C_{db}+C_{gb})}\, sC_{gb} \quad (3)$$

Small signal gain is defined as

$A_i = \frac{I_o}{I_i}$, and for unity gain I_0=I_i, we obtain (4)

$$f_T = \frac{g_m+g_{mb}}{2\pi(2C_{gd}+C_{gs}+C_{gb})} \quad (5)$$

From(5), it is observed that bandwidth can be improved by increasing the transconductance. In the composite transistor, shown is in Fig.3, a source follower is used between the gate and body terminal of conventional DTMOS which leads to higher transconductance and bandwidth.

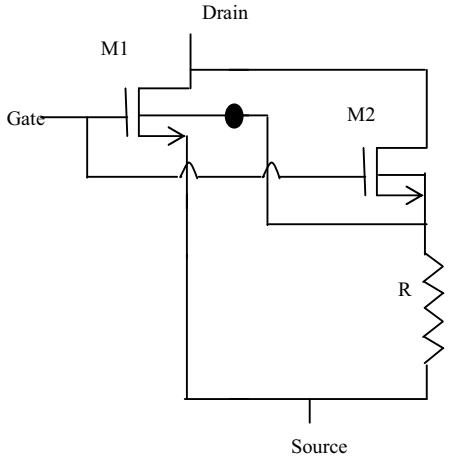

Fig. 3. Composite transistor consisting of DTMOS transistor and source follower

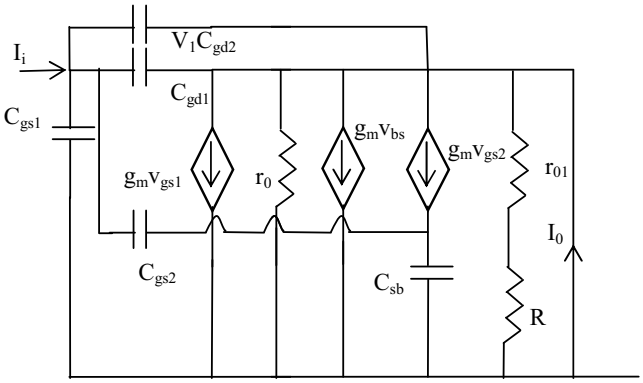

Fig.4. Small signal model of composite transistor

Analysis of Fig.4 gives following expressions

$$I_o = V_i\left(\frac{1+s\frac{C_{gs2}}{g_m}}{K}\right)\left(-\frac{1}{r_o} + g_{mb} - g_m\right) + V_i(-sC_{gd2} - sC_{gd1} + 2g_m) \quad (6)$$

where $K = \frac{1}{g_m}\left(sC_{sb} + \frac{1}{R} + sC_{gs2}\right) + 1$

$$I_i = V_i s\left(C_{gd1} + C_{gs1} + C_{gd2} + C_{gs2}\right) - \left(sC_{gs2}\right)V_i\left(\frac{1+s\frac{C_{gs2}}{g_m}}{K}\right) \quad (7)$$

From (4), we obtain

$$f_T = \frac{3g_m+g_{mb}}{2\pi(8C_{gd}+C_{gs}-2C_{sb})} \quad (8)$$

Comparing (5) and (8), it is observed that in proposed circuit total transconductance increase which would improve bandwidth also.

III. PROPOSED DIFFERENTIAL AMPLIFIER

The most important analog building block is a differential pair. It is the input stage of an operational amplifier and most integrated filters. The usefulness of the differential pair stems from two key properties. First, cascades of differential pairs can be directly connected to one another without interstage coupling capacitors. Second, the differential pair is primarily sensitive to the difference between two input voltages, allowing a high degree of rejection of signals common to both inputs. Hence differential amplifier has become dominant choice in low noise and high performance analog and mixed-signal circuits[10].

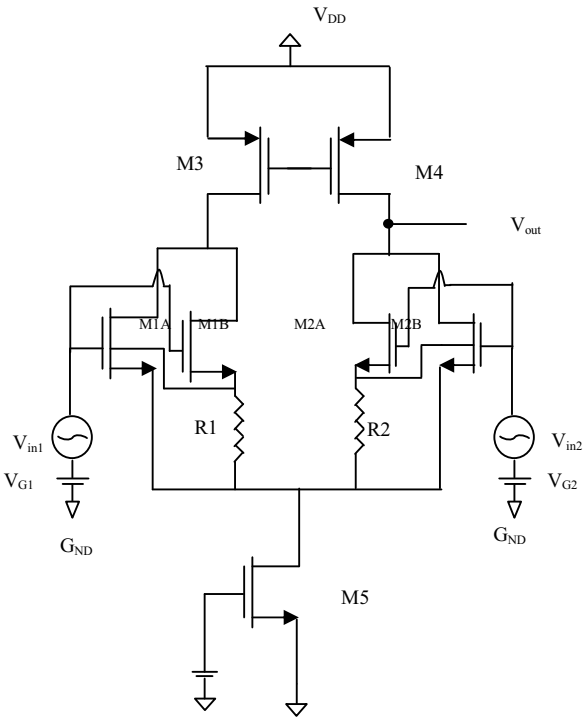

Fig.5 Proposed Differential Amplifier

Implementation of proposed differential amplifier using composite transistor is shown in Fig.5. In this circuit M1A, M1B forms composite transistor and another composite transistor is formed by M2A, M2B transistor. Direct use of current mirror as a load for a differential stage, leads to the self biasing of circuit in Fig.5. Also self biasing provides a double-to-single conversion. The output can be taken from one single output node, yet is functionally a differential output.

IV. SIMULATION RESULTS

All the circuit in have been designed in 180 nm CMOS technology to prove the validity of the idea. Fig.6 shows frequency response of composite transistor. As observed from the response, -3dB frequency of conventional DTMOS transistor is obtained as 2.325 GHz and for composite transistor -3dB frequency is obtained as 9.453 GHz. Thus use of source follower extends the bandwidth by a factor 4.065.

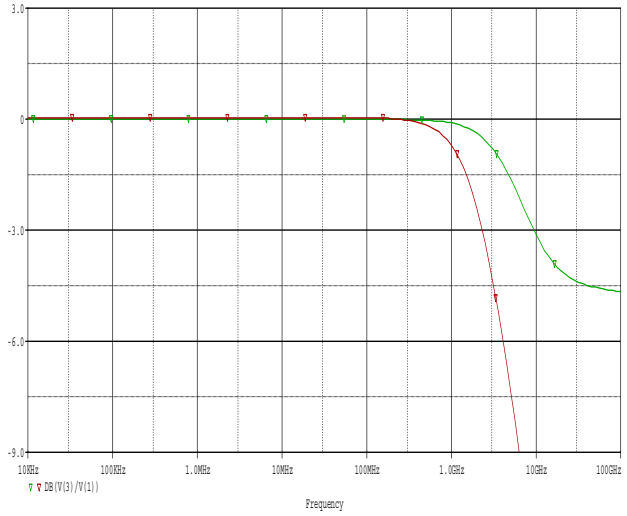

Fig.6 Frequency response of composite transistor

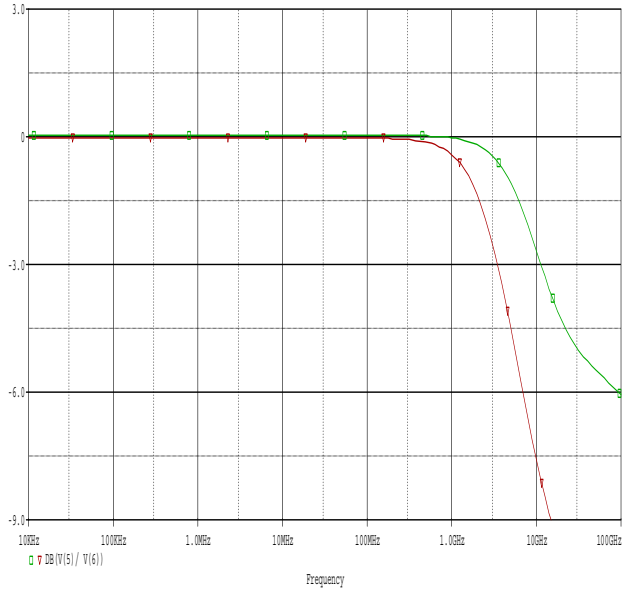

Fig.7 Frequency response of proposed differential amplifier

Fig.7 shows frequency response of proposed differential amplifier using composite transistor. As observed from the response, -3dB frequency of differential amplifier using conventional DTMOS is obtained as 2.325 GHz and for proposed differential amplifier -3dB frequency is obtained as 11.676 GHz. Thus use of composite transistor extends the bandwidth of differential amplifier by a factor 3.364. Table.1 shows comparison of various bandwidth extension ratio (BWER) of conventional and proposed circuits.

Table.1 BWER in conventional and proposed circuits

Parameter	**Transistor**	**Differential Amplifier**
-3dB frequency (GHz)	DTMOS: 2.325	Using Conventional DTMOS : 3.470
	Composite : 9.453	Using Composite transistor: 11.676
BWER	4.065	3.364

Fig.8 shows simulated power consumption in conventional DTMOS transistor and total 0.523 µW power is consumed. Fig.9 shows simulated power consumption in proposed DTMOS transistor and total 1.0362 µW power is consumed. This small increase in power dissipation is mainly because of increase in transistors in the proposed circuit. But this drawback as compared to the advantages achieved using source follower is not of much significance. Table.2 shows comparison of various parameters of conventional DTMOS and composite transistor.

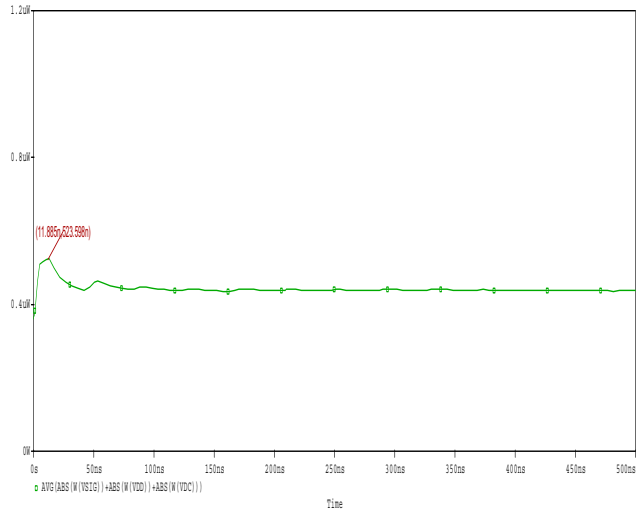

Fig.8 power consumption in conventional DTMOS transistor

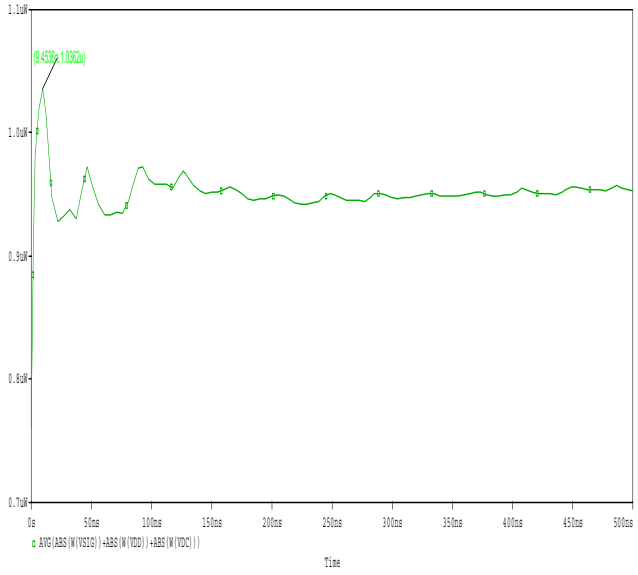

Fig.9 Power consumption in composite transistor

Table.2 Comparison of conventional DTMOS and composite transistor

Parameter	**Conventional DTMOS**	**Composite transistor**
Theoretical Bandwidth	$f_T = \frac{g_m+g_{mb}}{2\pi(2C_{gd}+C_{gs}+C_{gb})}$	$f_T = \frac{3g_m+g_{mb}}{2\pi(8C_{gd}+C_{gs}-2C_{sb})}$
Simulated Bandwidth (GHz)	8.83	28.18
Threshold Voltage (V)	0.322	0.441, 0.441
Power Dissipation (µW)	0.523	1.0362
Rise Time (ns)	5.129	3.684
Transconductance	$5.83x10^{-5}$	$2.2x10^{-5}$, $2.11x10^{-5}$

V. CONCLUSION

In this paper we have proposed to increase the bandwidth of differential amplifier using a composite transistor consisting of conventional DTMOS and source follower. The proposed approach increases the transconductance and thereby improving bandwidth. The proposed differential amplifier has excellent frequency response when compared to the conventional version. Although use of additional transistor may increase slightly the power consumption of circuit but advantage obtained in terms of higher bandwidth is more

significant. Thus the proposed differential amplifier could be very well applicable for low power RF analog domains.

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