Analysis of Low Power 1-bit Adder Cells using different xor-xnor gates

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***Abstract*— Addition is the basic arithmetic operation used in many VLSI circuits. Reduction in power dissipation of 1 bit adder cell will improve the performance of most of electronic devices. In this paper, 1 bit adder cells were analyzed with respect to supply voltage, temperature, width and length variation of all transistors in circuits. The 1 bit adders were designed using 10, 8 and 6 transistors using different equations of sum and carry. The adder designs considered in this paper are SERF adder, 13A adder, CLRCL adder, 8T adder and 6T adder. The comparison was done with respect to power, delay and area. The adder designs were checked for their robustness by varying supply voltage and temperature. The simulations were carried using OrCAD PSpice in 180nm technology with 1.8V supply voltage. Simulation results showed that SERF adder has lowest power dissipation of all adders. Delay of Sum signal was lowest in CLRCL adder and delay of Carry signal was lowest in 13A adder. The 6T adder was found to be best when area was considered as it is designed using less number of transistors as compared to all other adder designs. The adder designs can be chosen according to our design considerations.**

Keywords—Pass Transistor Logic (PTL), Complementary Pass transistor Logic (CPL), Static Energy Recovery Full (SERF), Complementary and Level Restoring Carry Logic (CLRCL)

I. INTRODUCTION

The advancements in VLSI technology have contributed to portable and handheld devices. Mobiles, laptops and other handheld devices need systems with low power dissipation. All sensor networks want their systems have long battery life. The adder is the basic building block in many VLSI applications such as DSP, cache memory and multipliers. The conventional 28 transistor 1-bit adder, which is designed using PMOS pull up and NMOS pull down networks. The delay in 28 transistor conventional adder is best when delay is taken into consideration with respect to all other adders but power dissipation and transistor count is very high. There is demand for compact low power devices in the market. To achieve compactness and low power consumption, we need to reduce number of transistors.To achieve low transistor count pass transistor logic (PTL) is used. Pass transistor logic reduces transistor count when compared to CMOS and CPL[8]. The main drawback of PTL is threshold voltage loss. The logic '1' in NMOS transistor is never be equal to the value of VDD and logic '0' is never equal to the value of GND. The pass transistor logic can be used in designing larger circuits where threshold voltage loss is not major concern. We have 10 transistor 1 bit adders like Static Energy Recovery Full adder(SERF), 13A adder, Complementary and Level Restoring Carry Logic(CLRCL) adder. The 8T adder is also available which is designed using three multiplexers and one inverter. We have a new 6T adder which is designed using only 3 multiplexers. Each multiplexer is designed using 2 transistors.

I. REVIEW

One bit addition has got three inputs A,B and Cin. The outputs of adder are Sum and Carry. They are generated using basic equations as in (1) and (2).

$$Sum = A \oplus B \oplus Cin \quad (1)$$

$$Cout = (A \cdot B) + (A \cdot Cin) + (B \cdot Cin) \quad (2)$$

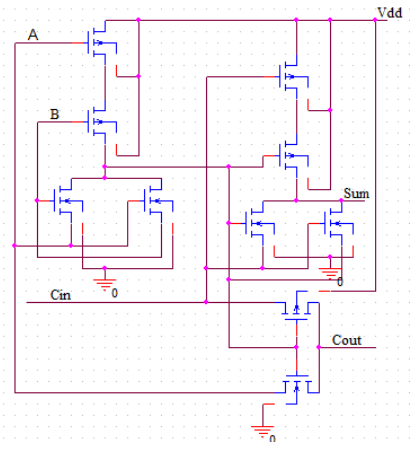

Fig. 1. SERF full adder design.

Four type of 10 transistor adders are reviewed in this section. All are designed using pass transistor logic (PTL). The first type of adder is SERF (Static Energy Recovery Full) adder[1]. In this circuit the charge which is drained during logic low is reused. It is used as input signal to control the gates of transistors. There is no direct path to ground. Hence the power dissipation due to short circuit current is completely reduced. Thus static energy is recovered. SERF adder therefore

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consumes less power than other non energy recovering adder designs. In non energy recovering adders, the charge in load capacitance is drained through ground during logic low. The main advantage of SERF adder is that it does not need any inverting inputs. The SERF adder as shown in Fig. 1 can be designed by rewriting Sum and Carry equations as in (3) and (4).

$$Sum = A \odot B \odot Cin \quad (3)$$

$$Cout = (A * (A \odot B)) + (Cin * (A \oplus B)) \quad (4)$$

The second type of 10 transistor 1 bit full adder reviewed is 13A adder[2]. In this paper total of 41 different adders are simulated and analyzed. The 41 transistors are designed using different combinations of XOR and XNOR gates such as INV XOR, INV XNOR,P-/G-XOR, P-/G-XOR, SER XOR and SER XNOR as shown in Fig. 3 and Fig. 4 of reference paper [2]. Different Cout modules are also used in different adder designs like multiplexer, double PMOS and double NMOS as shown in Fig. 6 of [2]. Out of 41 adders 13A adder comes out as best when compared with respect to low power and delay. 13A adder is built using SERF XNOR and INV XNOR. The Cout is designed using multiplexer.This one bit adder is designed as shown in Fig. 2 using equations (3) and (4).

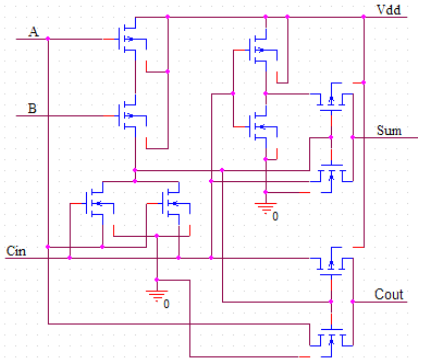

Fig. 2. 13A full adder design.

The third type of 10 transistor adder reviewed here is CLRCL (Carry and Level Restoring Carry Logic) adder[3]. The main disadvantage of pass transistor logic is reduced output voltage swing. An effort is made here to restore voltage swing. Two inverters and three multiplexers are used in the design. One of inverters act as buffer which speeds up the carry propagation in the circuit, thus reducing the delay. The main advantage of inverter circuits here is they act as level restoring logic.The other inverter provides complemented output of carry signal Cout. The output voltage swing of Sum and Carry signal is (Vdd-|Vt|). The main drawback of CLRCL adder is it requires inverted input signal Cin_bar which was not case in previous adder designs mentioned above.The CLRCL adder can be designed as shown in Fig. 3 by rewriting Sum and Carry equations as in (5) and (6).

$$Sum = (A \oplus Cin) * \overline{Cout} + (A \odot Cin) * B \quad (5)$$

$$Cout = (A \oplus Cin) * B + (A \odot Cin) \quad (6)$$

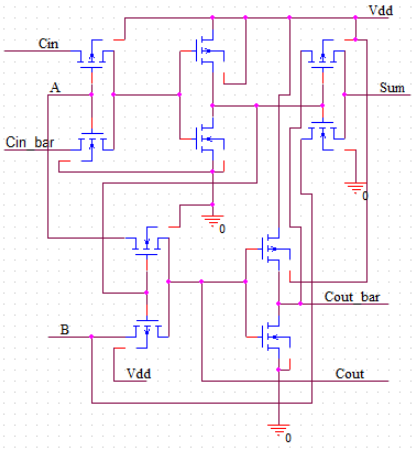

Fig. 3. CLRCL full adder design

The last type of 1 bit adder reviewed in this section is 8T adder[4]. It is built using three multiplexers and one inverter. The inverter in the circuit speeds up propagation of Cout and also provides complemented Cout signal required for generation of Sum. The 8T adder is designed as shown in Fig. 4 as in equations (5) and (6). The xor gate is replaced by xnor gate. So the need for inverter is avoided. This reduces the transistor count to 8. The simulation results show that the output voltage swing of 8T adder is not as good as CLRCL adder. One of inverters is reduced in 8T adder design. The 8T adder also requires inverting input Cin_bar as in the case of CLRCL adder. The only advantage of 8T adder is that transistor count is reduced to 8 from 10. The same equations used for CLRCL adder is used here.

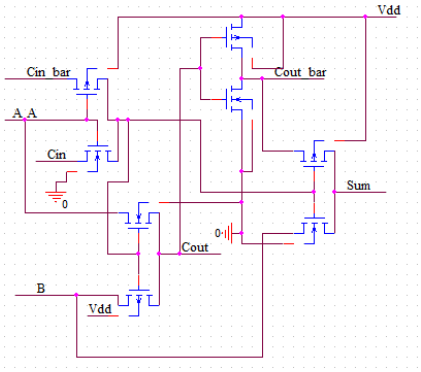

Fig. 4. 8T full adder design.

II. NEW 6 TRANSISTOR ADDER

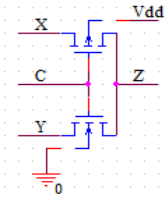

Fig. 5. Multiplexer design

The 6T adder is designed using three multiplexers only. Each multiplexer is designed using only two transistors as shown in Fig. 5.

The multiplexer can be used as both XOR and XNOR gate. In previous designs of 10 transistor adder the XOR/XNOR gates were designed using four transistors. So transistors in design were more. 6T adder uses three multiplexers in its design. In today's world all VLSI devices need to be compact as portability is main design consideration. This 6T adder is best suited for such applications. The output of MUX1 signal is used as select signal in MUX2 where Cin and Cin_bar are input signals. MUX2 generates Sum output. The output of MUX1 is also used as select signal for MUX3 where Cin and A are input signals. The output of MUX3 is carry signal Cout. These can be designed as shown in Fig. 6 by rewriting Sum and Carry equations as in (7) and (8)

$$Sum = (A \odot B) * Cin + (A \oplus B) * \overline{Cin} \quad (7)$$

$$Carry = (A \oplus B) * Cin + (A \odot B) * A \quad (8)$$

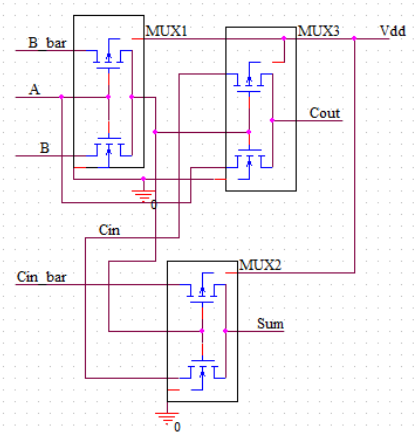

Fig. 6. 6 transistor adder design

MUX1 is used to generate (A⊙B) signal. It is used as control signal in both MUX2 and MUX3. MUX2 is used to generate Sum signal and MUX3 is used to generate carry signal. The inverter used in 8T adder is eliminated and it reduces number of transistors to 6.

III. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

Simulations were done using OrCAD Pspice through netlisting. The simulations were carried out in 180nm technology with power supply of 1.8V. Transient analysis was done at frequency of 100MHz and load capacitance of 100fF. The total power dissipation of all adders were obtained. The total power includes switching power, leakage power and short circuit power dissipation. The power dissipation due to short circuit is not present in case of SERF adder. So power dissipation SERF adder is less compared to all other adder designs. This is evident from simulation results. When simulations were carried out using OrCAD Pspice power dissipation results were lesser than as shown in previous papers. The power dissipation of 8T adder is not less than all other adders as claimed in paper [4]. Propagation delay of Sum and Carry were calculated. The propagation delay is the time between 50% input signal to 50% of output signal. Delay is measured between fastest changing input and fastest changing output. Total power dissipation, delay and transistor count of each adder design as shown in TABLE I .

TABLE I. PERFORMANCE COMPARISON OF ALL ADDERS

Metric	SERF adder	13 A adder	CLRCL adder	8T adder	6T adder
Total power Dissipation (nW)	0.305	0.483	2.76	0.347	0.594
Delay for Sum (ps)	11.375	18.25	10	19.75	21.5
Delay for Carry (ps)	21.75	9.6	28	32.125	20.75
Transistor Count	10	10	10	8	6

Simulation results of TABLE I shows that the power dissipation of SERF adder is low among all adders as total power dissipation is only due to switching power and leakage power dissipation. The delay for Sum signal of CLRCL adder is lesser than all other adders as in Fig. 7. This is due to the fact that there is inverter in path which will act as buffer and reduces the propagation delay for Sum. The delay for Carry signal of 13 A adder is very less as compared to all other adders as in Fig. 8. When we consider number of transistor the 6T adder has got lowest transistor count. This reduces total area of 1 bit adder. The width and length of in transistors are modified to obtain low power dissipation. The width of transistor is inversely proportional to the threshold voltage loss in designs. As we increase the width threshold loss can be reduced and output voltage swings can be obtained [10]. The increase in width of transistor also reduces propagation delay. Inverter has ratio of W/L=4/1 and 2/1 for PMOS and NMOS respectively. The 2-1 MUX has ratio of W/L=6/1 and 3/1 for PMOS and NMOS respectively. The 4 transistor XOR/XNOR gates were designed with PMOS of ratio W/L=8/1 and NMOS of ratio W/L=2/1. This will help us to optimize all adder designs for lower propagation delay with better output voltage swings.

The supply voltage is important parameter when we consider power dissipation as it has quadratic relation. The supply voltage was varied as 5v,3.3v and 1.8v. The power dissipation of all adder designs was calculated for all supply voltages. The Fig.9 shows that SERF adder is better than all adder designs and has got lowest power dissipation. It is followed by 13A adder and 6T adder. The 8T adder has got lesser power dissipation than CLRCL adder when supply voltage is 1.8v,but not at supply voltage of 3.3v and 5v.

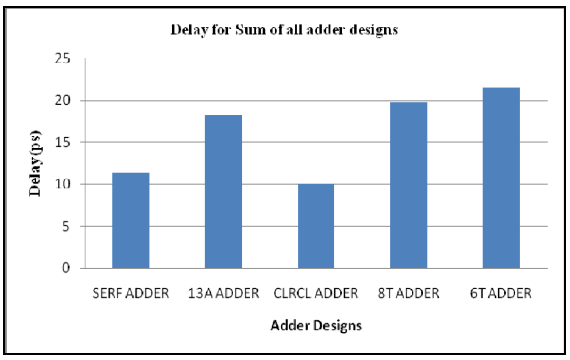

Fig. 7. Comparison of delay for Sum signal of all adder designs

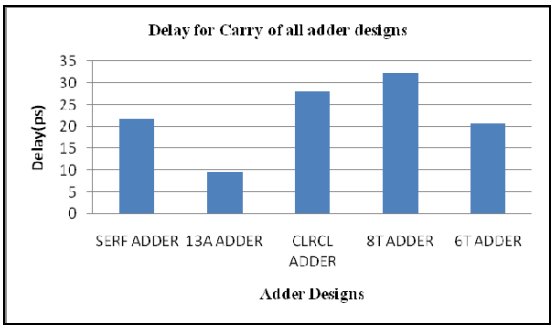

Fig. 8. Comparison of delay for Carry signal of all adder designs

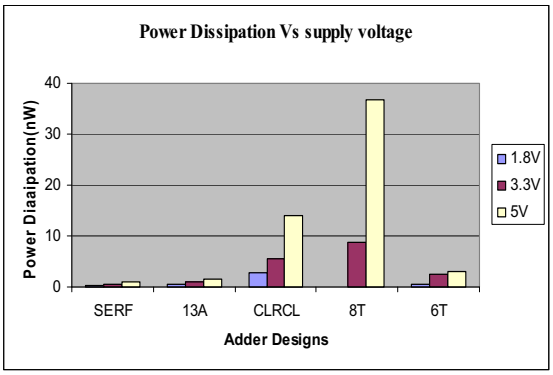

Fig. 9. Comparison of power dissipation of all adder designs for various supply voltages

Next the adder designs are analyzed for their performance at different temperatures. The designs were simulated at various temperatures to check their robustness[11]. The adder designs were simulated at temperatures of 10,20,30,40 and 50 degree Celsius. The tabulated results are in table II.

When the TABLE II is analyzed, it is observed that as we increase temperature from 10 to 50 degree Celsius the power dissipation also increases in all adder designs. The power dissipation is directly proportional to long battery life. The cooling system has to be effective also. In order to have robust system we have to design adders at specified range of temperatures. Analysis of power dissipation of all adder designs can be observed as in Fig.10.

TABLE II. COMPARISON OF POWER DISSIPATION OF ALL ADDER DESIGNS AT VARIOUS TEMPERATURES

Metric	**Power dissipation(nW)**				
Temperature (deg Celsius)	SERF Adder	13A adder	CLRCL adder	8T adder	6T adder
10	0.154	0.223	1.88	0.162	0.263
20	0.231	0.353	2.31	0.254	0.428
30	0.343	0.550	2.99	0.395	0.682
40	0.505	0.841	3.96	0.605	1.06
50	0.734	1.26	5.28	0.912	1.61

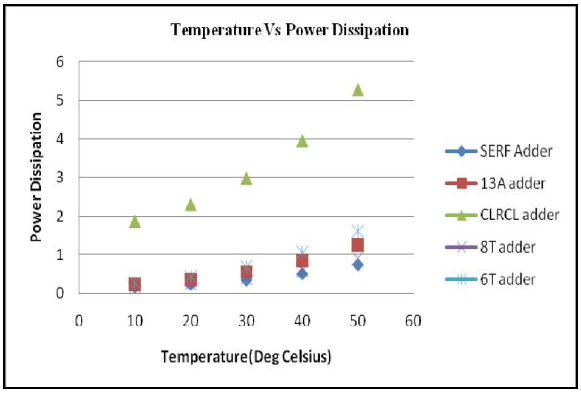

Fig. 10. Power Dissipation of all adders with variation of temperature

IV. CONCLUSION

In this paper, extensive simulations were carried out using OrCAD PSpice to evaluate and compare the performance of SERF adder, 13 A adder, CLRCL adder, 8T adder and 6T adder. Performance analysis was done with respect to various supply voltages and temperatures. The SERF adder has lowest power dissipation at supply voltage of 1.8v. The delay for Sum of CLRCL adder is lesser than all other adders but delay of carry in 13A adder design stands out best. All designs will definitely help to build larger circuits such as multiple bit adders and multipliers where threshold voltage loss is not a major concern. The adder designs can be chosen according to the design specifications. If compactness is the design issue and we want our adder design to consume lesser area then 6T adder can be used. If power dissipation is a major concern then SERF adder can be used. If delay is a major consideration then CLRCL adder or 13 A adders can be used.

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