Debug Challenges for UTMI Low Pin Interface (ULPI) PHY in Nano Scale Technology

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Abstract—**Real world communication are analog in nature whereas data processing happens in digital domain. This leads to generation of Mixed Signal design. With reference to USB, ULPI PHY serves as mixed design component that is present in most of today's gadgets. Because of its high speed and complexity, there is a need to check the individual design features of the ULPI PHY IP, which are hard to validate when the embedded in a System on Chip. The limitation comes from the fact that only a limited number of signals can be probed at SOC level.**

This paper describes the debug challenges and techniques used to validate these features before the IP goes into SOC.

Keywords—ULPI; USB; nano scale; Low Pin Interface; UTMI

I. INTRODUCTION

New products on smaller technologies are required to meet the cost and demand for the semiconductor industry. This requirement poses serious challenges for ULPI PHY to meet the strict specifications for USB2.0 with scaling in feature size [1] [2]. Further it needs to be properly validated before going into any product or SoC. The new designs are more prone towards bugs so this leads to the idea of standalone setup where all the design features of ULPI PHY can be validated [5]. As soon as IP matures it is ready for the final product.

Announced on March 1, 2004, the ULPI specification provides a low-pin, low-cost, small form-factor transceiver interface for any USB application [6]. Using the existing UTMI+ specification as a starting point, the ULPI working group reduced the number of Link to PHY interface to 12 or 8 signals, with support for all the features needed by USB peripherals, hosts, and OTG [3] [4].

This paper is divided into four sections. Section II describes the need for standalone ULPI-PHY validation. Section III highlights some of the debug challenges and case studies encountered during the testing. Section IV summarizes the paper with recommendations for future work.

II. NEED OF UTMI LOW PIN INTERFACE PHY VLAIDATION

Designers all over the world are facing increasing pressure to design smaller products, in less time, and at lower cost. At the same time, as smaller deep sub-micron processes are introduced, integrating the physical layer analog circuitry required by technologies such as USB and On-The-Go (OTG) is a complex task that has become a technical challenge, requiring more man-hours, more investment, and more silicon spins. A better way would be to have a ULPI PHY standalone chip first where all the features of ULPI PHY could be tested across process, voltage and temperature.

If a ULPI PHY directly goes into SoC without extensive coverage prior to system level validation of SoC then it would have the following constraints in validation.

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- Many PHY signals would not have been brought out in SoC environment, which would make it difficult to test all the functionalities of PHY. For example Full Speed common mode receiver sensitivity issue (REF- Section A)
- Due to PHY-controller limited configurations there is no possibility to test all scenarios specially the negative ones. For example Full Speed Time Out issue (REF-Section B)
- If there is any issue, first it needs to be identified and sorted out as to whether the issue belongs to controller, PHY or SoC environment, but isolating the issue is a cumbersome task as many more variables are present in SoC environment (e.g. Pads, System bus, different clock domains, etc.)
- Due to the complexity of system level testing and less debug capability, it would be very difficult to identify the root cause of the failure, which in turn could delay the time to market and lower quality product.

A. Full Speed Time Out Error

A device expecting a response to a transmission will invalidate the transaction if it does not see start-of-packet (SOP) transition within timeout period after the end of the transmission (after SE0-to-J state transition in the EOP). This can occur between an IN token and the following data packet or between a data packet and the handshake packet. The device expecting the response will not time out before 16 bit times but will timeout before 18 bit times (measured at the data pins of the device from the SE0-to- J transition at the end of the EOP).Time out period should be 18 full speed bit time but in our case it is more than 70 full speed bit time [10].

This time-out issue was captured during standalone validation of ULPI PHY, which was fixed in the design.

B. Full Speed Common mode receiver Sensitivity

Compliance test doesn't specify any test for Full Speed or Low Speed (FS/LS) differential receiver sensitivity. FS/LS differential receiver has an input sensitivity of at least 200mV amplitude and dc offset between 0.8 and 2.5 volts common mode. If this specification is somehow not met in the design, it is impossible to test it in SoC level testing unless there are some design exposes were implemented. Exposing internal signals require additional silicon area and increases complexity of SoC architecture. The above described FS receiver sensitivity issue was found during standalone testing of ULPI PHY.

III. CHALLENGES AND CASE STUDIES

This section presents a few issues caught during standalone PHY validation. Earlier capture of the issues and root cause identification resulted in robust PHY and eliminated re-spins in many SoC's

A. Full Speed Crossover Voltage& Eye Diagram Issue

While performing Signal Quality testing for ULPI PHY in Full Speed, far end device configuration, two issues were found – crossover voltage and failing eye diagram [7].

It was found that crossover voltage was not meeting the required spec (2.0V at -40C at 3.6V) and eye diagram was failing (Figure 1(a)) & (Figure 2(a)). For USB compliance the crossover voltage should be between 1.3V to 2.0V.

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Population	Status
Eye Diagram Test	-	-	-	-	-	-	-	Pass
Signal Rate	11.89050Mbps	12.06564Mbps	11.99933Mbps	0.0000bps	56.70788kbps	11.99058Mbps	30	Pass
Crossover Voltage	1.836175 V	2.121979 V	1.979175 V	285.8040 mV	114.9681 mV	1.982345 V	20	Conditional Pass
EOP Width	-	-	166.8088ns	-	-	-	1	Pass
Consecutive Jitter	-500.3399ps	532.5283ps	25.83809ps	1.032868ns	278.6176ps	272.4146ps	19	Pass
Paired JK Jitter	-295.3203ps	270.7360ps	41.57810ps	566.0563ps	230.4106ps	217.3330ps	7	Pass
Paired KJ Jitter	-358.9266ps	271.5950ps	-2.700521ps	630.5216ps	248.4504ps	230.0362ps	7	Pass
Falling Edge Rate	361.4742 V/us	420.2527 V/us	389.2877 V/us	58.77845 V/us	15.25969 V/us	389.5724 V/us	21	Pass
Rising Edge Rate	405.2980 V/us	464.9612 V/us	437.7998 V/us	59.66320 V/us	14.66519 V/us	438.0331 V/us	20	Pass

Fig. 1. (a) Highlighted Failing FS Cross Over Voltage

Both of the issues were fixed in design, the crossover voltage issue was fixed by reducing transmitter output current, which resulted in reduction of crossover voltage by 200mV. The eye diagram issue was fixed by changing the output driver for FS mode. These tests were done again in the subsequent test chip (ULPI PHY) where it was found to be working as expected. (Figure 1(b)) & (Figure 2(b))

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Population	Status
Eye Diagram Test	-	-	-	-	-	-	-	Pass
Signal Rate	11.97853 Mbps	12.02152 Mbps	11.99816 Mbps	0.0000b ps	13.39553 kbps	11.99736 Mbps	25	Pass
Crossover Voltage	1.419686 V	1.656071 V	1.547383 V	236.385 1mV	69.88950 mV	1.548862 V	16	Pass
EOP Width	-	-	166.8022 ns	-	-	-	1	Pass
Consecutive Jitter	-486.5900 ps	237.8390 ps	12.58860 ps	724.429 0ps	199.0725 ps	192.7339 ps	15	Pass
Paired JK Jitter	-130.0950 ps	417.6540 ps	137.7507 ps	547.748 9ps	195.9939 ps	222.9488 ps	5	Pass
Paired KJ Jitter	-52.04543 ps	288.7029 ps	47.51929 ps	340.748 4ps	137.7085 ps	132.0189 ps	5	Pass
Falling Edge Rate	249.5836 V/us	286.3554 V/us	270.6079 V/us	36.7718 4 V/us	9.937601 V/us	270.7789 V/us	16	Pass
Rising Edge Rate	1.000000 V/us	253.7978 V/us	224.9007 V/us	252.797 8 V/us	60.35479 V/us	232.3690 V/us	16	Pass

Fig. 1. (b) FS Crossover Voltage after debug and fix.

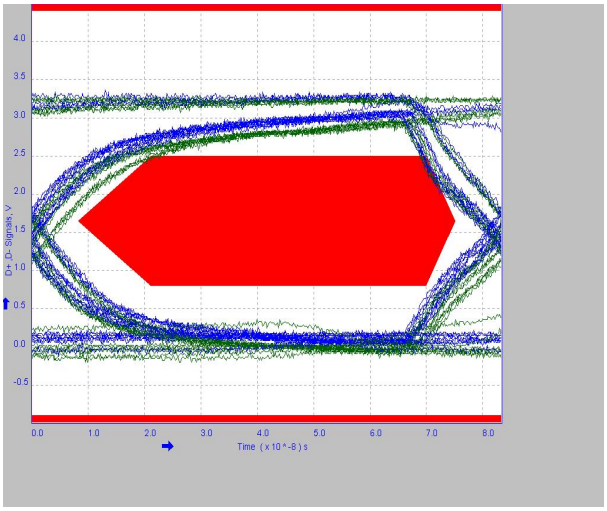

Fig. 2. (a) FS eye diagram failure.

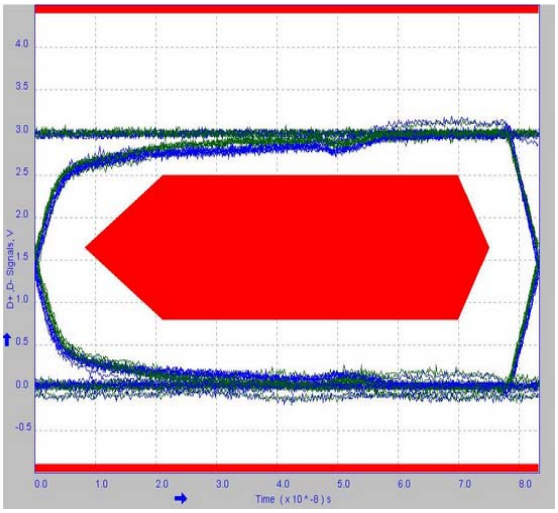

Fig. 2. (b) Passing FS eye diagram after debugging and fix

B. *HS High Speed Eye Diagram Failure*

A serious signal quality issue was observed during ULPI PHY testing in High Speed Host mode. The eye diagram in Figure 3(a) shows the issue. The eye diagram was passing at room temperature and cold temperature but failing/marginally passing at hot Temperature [8].

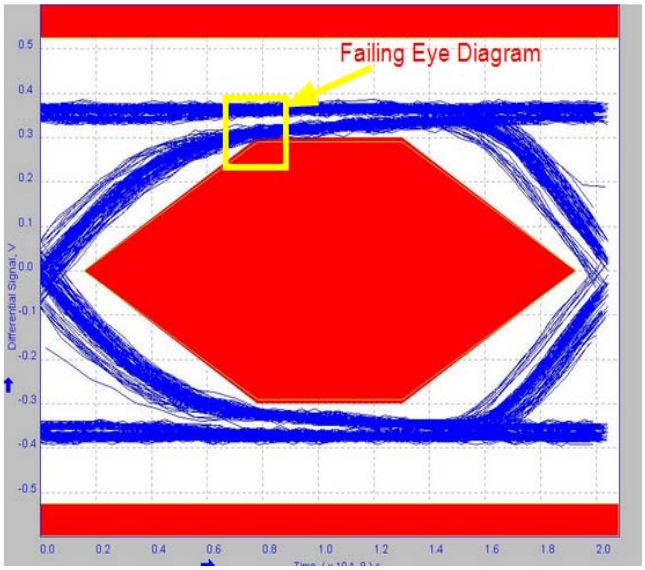

Fig. 3. (a) Failing HS Eye Diagram.

Fig. 4.

Later this issue was also seen during High Speed device mode and showed a worse eye diagram than Host mode.

After debugging, it was determined that o/p driver current was lower than the expected value, which was increased to have a passing eye diagram. (Figure 3(b)).

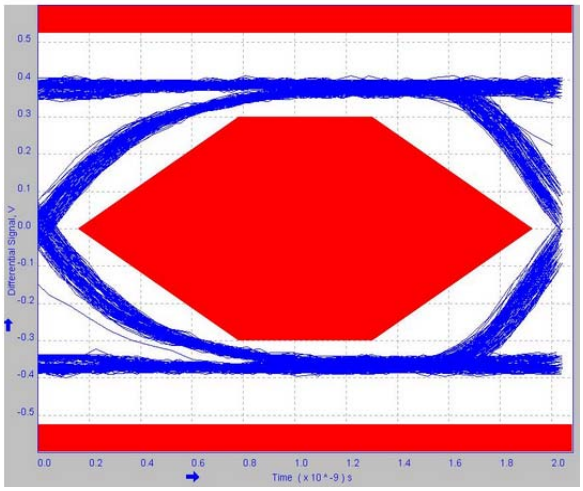

Fig. 3. (b) Passing HS Eye Diagram after debugging.

C. HS Transmit Data Signal

In our experiment, there was a problem in obtaining the HS eye diagram because the HS signals on DP and DM were nearly half of the actual amplitudes as shown in Figure 4 (a) [9].

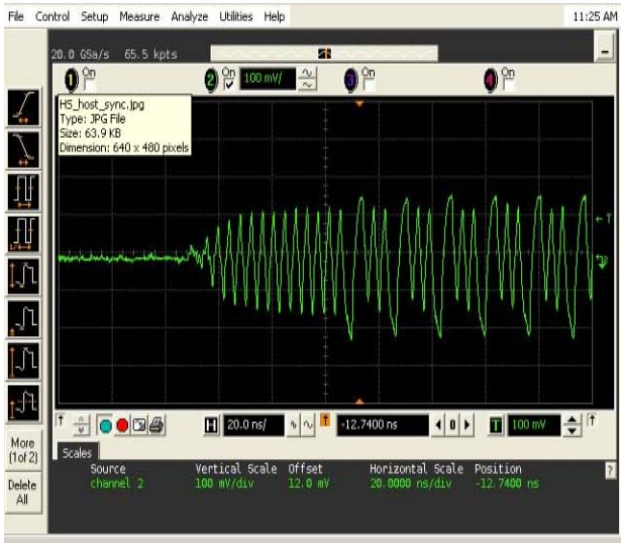

Fig. 4. (a) HS transmit differential data before debugging.

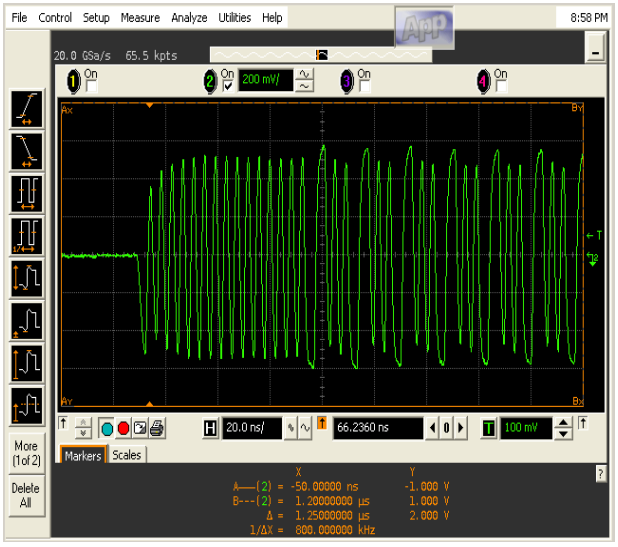

Fig. 4. (b) HS transmit differential data after debugging.

One common 5V supply was used to generate different supplies for USBPHY block. After checking, it was determined that all the supplies of 1.8V, 3.3V were proper. FS, LS transmitter and HS Receiver were working properly, but HS transmit level was incorrect, causing eye diagram failure. After debug on the standalone ULPI validation setup, it was found that by increasing around 500mv to one of the 1.8V (five 1.8V supplies in the design) supply, HS signals reached the required amplitude and HS eye diagram could be taken as shown in Figure 4 (b). This change in supply voltage could only be performed by standalone validation.

D. Transmit Error

In cases when link forces data 0xFF for more than one clock cycle on the bus, PHY will automatically generate an FS transmit error by sending a minimum of 8 consecutive 1's on the USB bus.

The main problem was to observe this transmit error on USB bus with legacy setup used in validation as link can't send this type of data for more than one clock cycle in traditional setup.

However, at our validation setup, transmit error can be observed by writing code in FPGA in such a way that this scenario can be created.

IV. Conclusion

By doing extensive stand alone validation of ULPI PHY many issues were discovered which were hard to identify in SOC and system level environments. This resulted in robust ULPI PHY, which will prevent many SoC re-spins and customer issues later in the product life cycle.

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