Design of FIR Filter Using FCSD Representation

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***Abstract*—This paper presents design and implementation of a sixteen order efficient FIR filter for wireless communication system. In this work, factored canonical signed digit representation (FCSD) is used in order to reduce the design complexity as compared to canonical signed digit (CSD). We have replaced multiplication operation with add and shift method by representing coefficient in CSD and FCSD format for reducing the complexity of the system. FIR filter has been designed using an equiripple method in MATLAB and further synthesized on Spartan3E XC3S500E target FPGA device. Simulation results show that Symmetric FCSD based FIR filter offers 35.68% less number of slices as compared to the direct form filter structure and 8.355% less number of look up tables (LUT) as compared to CSD based filter.**

***Keywords*—DSP, FIR Filter, CSD, FCSD.**

I. INTRODUCTION

Digital FIR filter is one of the essential components in Digital Signal Processing (DSP) and communication system. With an explosive growth in mobile computing and multimedia applications, demand for low power and high speed DSP system has been increased. Digital filters are widely adopted in communication system for applications like channel equalization, matched filtering and pulse shaping to modify attributes of signal [1].Digital filter transforms digital representations of analog signals to remove noise and other unwanted signal components and shape the spectral characteristics of the resulting signal [2]. Digital filters are very superior in level of performance as they are highly accurate and stable as compared to analog filter which are very fast and have wide dynamic range in both amplitude and frequency. Moreover, digital architecture can be designed in field programmable gate array (FPGA) which operates at high data rate and low power [3]. So this reason makes FPGA ideal for high performance and low power DSP applications.

The FPGA is one of the best devices for hardware implementation of digital filters due to its fast progress in VLSI technology. But the main challenge of this paper is to design a digital filter with optimized power, area and delay [2, 5]. This paper focuses on the FIR filter due to its absolute stability and linear phase response.

The main components of digital filter consist of register banks to save samples of signals, adders to carry out sum operations and multiplier for multiplication of the filter coefficients with signal samples. Despite the fact that designing of digital filter seems simple but the design bottleneck is its multiplier block for speed, power consumption and FPGA chip area occupation [6]. The main drawback of FIR filter is the amount of computation required to process the input signal. Reduction in complexity of digital filter leads to high performance as well as low power design.

Complexity is mainly dominated by coefficient multiplication operation [7]. In order to reduce complexity, multiplication is replaced with simple operations such as addition, subtraction and shift and further filter optimization can be done by minimizing the number of adders. Multiple constant multiplication (MCM) operation provides maximum performance and minimum power consumption because of multiplication of same input by different set of coefficient [8-9].Various methods have been proposed earlier for optimization of MCM [3]. Hsiao et. al. have considered shift operation along with adders to form partial terms. A second approach is the use of CSD representation for the coefficients where coefficients are represented with minimal non-zero bits [10]. In the present work, we have used a modified CSD representation which is known as Factored Canonical Signed Digit (FCSD) in order to reduce the hardware complexity of the design.

The rest of the paper is organized as follows: an overview of FIR filter designing and structure is given in Section II. Section III describes CSD and FCSD method. Section IV discusses experimental and simulation results. Finally, Section V concludes the paper by summarizing the main contributes.

II. FIR FILTER

A. Theory

FIR filters are digital filter with finite impulse response. It can be represented in the form of a block diagram as shown below:

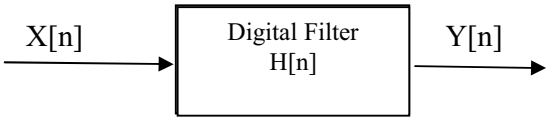

Fig. 1.FIR block diagram

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FIR filter is also known as non-recursive digital filters as they don't have feedback [2].It involves a convolution operation:

$$Y[n] = X[n]*H[n] \quad (1)$$

Linear time invariant (LTI) FIR filter can be described by the following difference equation

$$Y(n) = \sum_{k=0}^{N-1} H_K x(n-k) \quad (2)$$

Where N and H_k represents the length and coefficients of the FIR filter respectively [3].

Digital filter can be designed by calculating the filter coefficient on the basis of filter order, sampling frequency, pass band and stop band frequencies etc.[6]. Generally, power consumption and the amount of computation are directly proportional to filter order. Filter coefficient can be found with the MATLAB FDA tool. For optimization of area, power and delay in FIR filter, different approaches were introduced based on direct, transposed and symmetric architecture.

B. Structure

In Direct form, Signal samples are multiplied by filter coefficients and combined together in adder block. A modification over direct form is transposed structure. In transposed form, the shift register is not used which further optimize area and delay as compared to direct form [8].

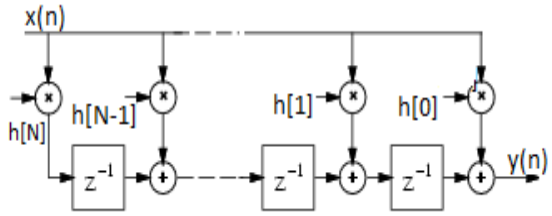

Fig.2. Transposed form of FIR filter

When the FIR system has linear phase, Impulse response satisfies either symmetric or asymmetric condition

$$H(n) = \pm h(N-n-1) \quad (3)$$

For this system multiplication has been reduced from N to N/2 for N even and to (N-1)/2 for N odd [8]. Therefore, linear phase symmetric structure further reduces the area, power and delay.

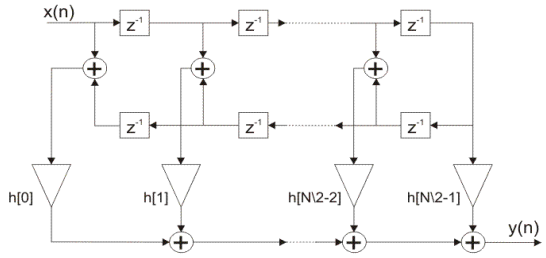

Fig.3.Symmetric direct form of FIR filter

C. Designing

Filter can be designed by different method including window functions, frequency sampling and equiripple method [7]. Table I lists the parameters of the low pass FIR filter and the corresponding magnitude response is shown in fig 4.

TABLE I. FIR Filter Design Parameter

Filter Parameter	Value
Design method	Equiripple
Order	16
Density factor	20
Sampling frequency	F_S = 48000 Hz
Passband frequency	F_{pass} = 9600Hz
Stopband frequency	F_{stop} = 12000Hz
Passband weight	W_{pass} = 0.1
Stopband weight	W_{stop} = 0.1

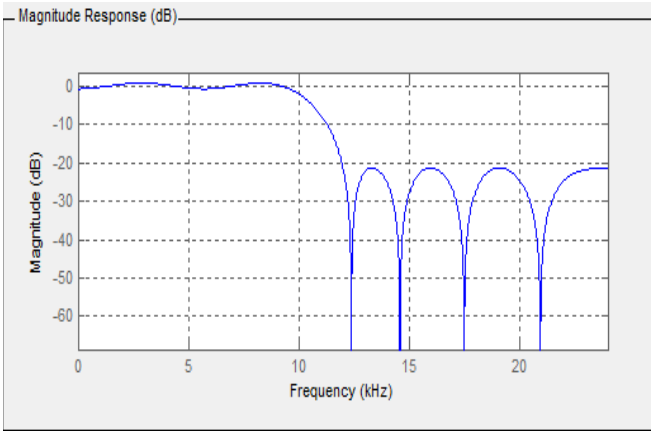

Fig.4. Lowpass FIR filter magnitude response

The calculated coefficients of the proposed FIR filter are given in table II. Coefficients are symmetric in nature which further reduces area and power consumption [5].

TABLE II. FIR Filter Coefficients

Coefficient Number	FIR Digital Coefficient
H[0]=H[16]	-0.043954858295096391
H[1]=H[15]	-0.035981065546366466
H[2]=H[14]	0.050699349043343445
H[3]=H[13]	0.030422136814391921
H[4]=H[12]	-0.036391465734247633
H[5]=H[11]	-0.096520567607945418
H[6]=H[10]	0.052875967350882083
H[7]=H[9]	0.30923012912837095
H[8]	0.4535420152702368

III. CSD AND FCSD METHOD

As multiplications make the filter designing complex due to its large area and power requirement, therefore, it has been replaced by add and shift operations or Common subexpression elimination (CSE) in which we use CSD or FCSD representation instead of binary representation. These representations are given below:

A. CSD

It is radix-2 signed digit system with weights {-1, 0, 1}. CSD representation is mathematically unique and independent of other constants [7]. Therefore it's not suitable for multiple constants. Coefficient can be represented in CSD code as given below:

$$X_{10} = \sum_{r=0}^{B-1} x_r 2^r \quad (4)$$

Where x_r = 0, 1 and -1

And -1 is denoted by $\bar{1}$

Properties

- CSD representation is a Signed Digit representation with minimal number of non-zero elements.
- Consecutive bits in a CSD representation can't be nonzero
- Nonzero elements guarantee the least number of adders.

This representation significantly reduces logic resources in synthesis and simulation. On average, CSD coding contains 33% fewer non zeros as compared to binary representation [9]. Product of adjacent two digits is zero. This property is termed as "property M". If signed digit representation of coefficient satisfies property M, then it is the CSD representation.

B. FCSD

Factored CSD algorithm is a slight modification over CSD. It replaces multiplier operation with shift and add operations on the basis of prime factors of the coefficients [4]. A combination of effective factorization and CSD representation of filter coefficient leads to a reduction in the number of adders which further reduces hardware cost. It provides a relatively greater reduction in filter area, but at the cost of decreased clock speed [4]. This technique is mainly used when a filter for wireless application is required. The Factored CSD algorithm is a trade-off between calculated complexity and convergence. Following example compares CSD and FCSD algorithm.

y = 217*x
= (11011001)*x % 217 in binary form
= (1001'001'1'1') *x % 217 in signed digit
= (256- 32-4-2-1) * x
= (x << 8) –(x << 5) – (x << 2) – (x << 1) – x

Cost of CSD = 4 adders

y = 217*x
= (7*31)* x
= (x << 3– x) *(x << 5 – x)

Cost of FCSD = 2 adders

It is concluded that, the number of adders has been reduced by using FCSD instead of CSD technique. Therefore we have used FCSD formulation for reducing filter complexity.

IV. RESULTS

This section presents the experimental and simulation results of implemented FIR filter. The result shows the enhanced performance in terms of speed, area and power consumption due to efficient utilization of embedded multiplier and LUT's inside the device. As filtering is a real time application, it uses combinational multiplier which increases speed in comparison with sequential multiplier [6]. Experimental and simulation results are given below:

A. Experimental results

Low power FIR Filter is designed with equiripple method in MATLAB for calculation of coefficients by using CSD and proposed FCSD Method. The filter can be designed in 3 structures, i.e. direct form, transposed and symmetric filter. Implementation cost has been computed in terms of multipliers and adders. It is shown in table III.

TABLE III. Performance Comparison of Structures

Design approach	Direct form	Transposed form	Symmetric form
No. of adder	16	16	17
No. of multipliers	17	17	9
No. of slice	1303	785	838
Flip flops	305	584	305
LUT's	2358	1499	1393
Frequency(MHz)	18.001	47.55	25.44
Min. period(ns)	55.553	20.94	39.308

Symmetric structure lowers the number of multipliers by half by folding the delay pipeline as compared to direct and transposed form.

B. Simulation result

FIR filter architecture has been designed and implemented on Xilinx Spartan3E XC3S500E with VHDL. The result realizes an FIR filter which can be operated at maximum frequency of25.44MHz by consuming 838 slices. The characteristics of proposed FPGA based FIR filter are summarized in table IV.

TABLE IV: Performance Comparison between CSD and FCSD

Parameter	CSD	FCSD
No. of slices	866	838
No. of flip-flops	305	305
No. of 4 input LUT's	1520	1393
Frequency (MHz)	26.483	25.44
Min. Period (ns)	37.76	39.308

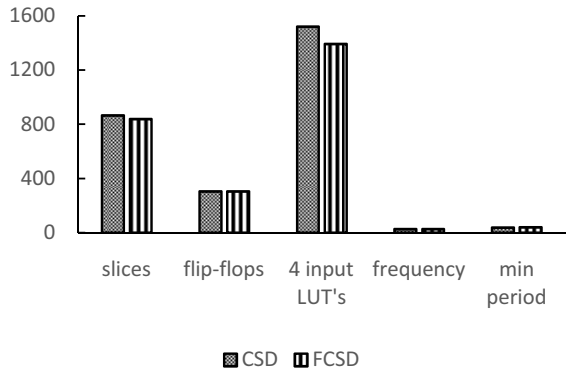

Fig.5. Bar graph representing CSD and FCSD comparison

Figure 5 represents the comparison of CSD and FCSD method in the form of bar graph. Simulation result of FCSD based FIR filter is shown in fig 6. The response of synthesized filter on FPGA is same as that of the simulated filter by MATLAB FDA tool box. As shown in table IV, Number of slices has been reduced from 866 to 838 in FCSD technique with the same number of flipflops. FCSD based FIR filter offers less number of look up table as compared to CSD technique. Although, the delay of FCSD based FIR filter is comparable to that of CSD based filter, however, the reduction in design complexity of FCSD based filter can be viewed as a possible alternative for circuit designer.

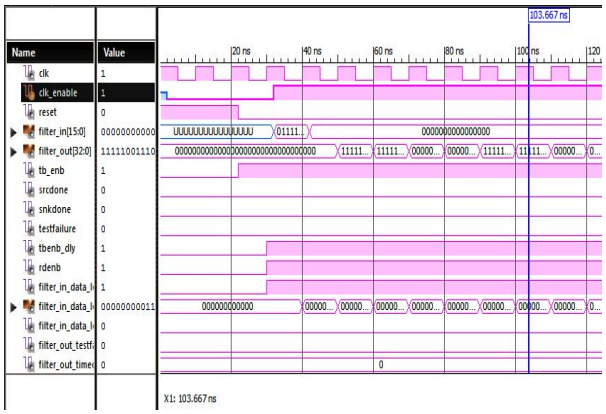

Fig.6. Simulation result of FCSD based FIR filter

V. CONCLUSION

FIR filter has been designed for 16 tap using FCSD representation for filter coefficients. After designing in VHDL it is further simulated on Xilinx Spartan3E based XC3S500E target FPGA device. The developed symmetric FIR filter requires 35.68 % less slices as compared to direct form FIR filter. The results show that FCSD based FIR filter can be operated at a maximum frequency of 25.44 MHz by consuming 838 slices, 305 flip-flops and 1393 LUT's. It is concluded that, use of FCSD representation in FIR filter can target significant reduction in design complexity when compared to CSD based FIR filter.

REFERENCES

[1] D. L. Maskell, "Design of Efficient Multiplierless FIR filters," *IET Circuits Device System*, vol.1, no. 2, pp. 175-180, May 2007.

[2] Michael D. Cilletti, Advance Digital Design with Verilog HDL, PHI learning, first edition,2003.

[3] S. Fu Hsiao and J. H. Zhang Jian, "Low Cost FIR Filter Designs based on faithfully Rounded Truncated Multiple Constant Multiplications," *IEEE Trans. on Circuits and Systems-II: Expression Briefs*, vol. 60, no. 5, pp.287-291, May, 2013.

[4] Mathworks, User guide filter design toolbox,version-2,2007.

[5] A. Nandi, A. K. Saxena and S. Dasgupta, "Design and Analysis of Analog Performance of Dual-k Spacer Based Underlap N/P-FinFET at 12nm Gate Length," *IEEE Trans. on Electron Devices*, vol. 60, no. 5, pp. 1529-1535, May 2013.

[6] F. Nekoei andY.S.Kavian,"Some Schemes of realization digital FIR filters on FPGA for communication applications,"*IEEE conf. on CriMiCo*, pp 616-619, Sep. 2010.

[7] R.Mahesh and A.P.Vinod,"A New Common Subexpression Elimination algorithm for realizing low complexity higher order digital filters," *IEEE Trans. On Computer Aided Design of Integreted Circuits and Sytems*, vol. 27, no. 2,pp. 217-229, Feb. 2008.

[8] Lingjuan Wu,Y. Cui and J. Huang, "Design and Implemenation of an Optimized FIR filter for IF GPS signal simulator,"*IEEE conf. on Microelectronics and Electronics*, pp 25-28, Sept. 2010.

[9] J. Proakis and D. Manolakis, Digital Signal Processing, fourth edition, 2008.

[10] R. Mahesh and A. P. Vinod, "New Reconfigurable Architecture for Implementing FIR filters with Low Complexity", *IEEE Trans. on Comp. Aided Design of Integreted Circuits and Sytems*, vol. 29, no. 2, pp. 275-275, Feb. 2010.