Design of a Stable Read-Decoupled 6T SRAM Cell at 16-nm Technology Node

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***Abstract*— This work presents a new single-port 6T SRAM cell with a single-ended read operation (read-decoupled) and shows significant improvement in read stability and write-ability as compared to the conventional 6T (CON6T) SRAM cell. Unlike the CON6T cell where the pull-up transistors are powered by the supply voltage (V_{DD}), the proposed cell has powered these transistors by the bitline driver. Another distinct feature of the proposed design is the presence of a PMOS transistor between the two storage nodes which is used during the write operation. The design metrics of proposed stable read-decoupled 6T SRAM cell are compared with those of the CON6T SRAM cell. The proposed cell shows 4× improvement in read static noise margin (RSNM) and 8% improvement in write static noise margin (WSNM) @ 700 mV.**

Keywords—SRAM; read-decoupled; read SNM; write SNM.

I. INTRODUCTION

As technology is advancing, the performance of microprocessors has improved significantly. But the operating speed of memory has not shown the level of improvement as shown by processor. To bridge this performance gap between processor and memory, silicon industry has developed on chip integration of semiconductor memory known as cache. Cache helps in transferring data in lesser time. Higher on chip integration provides the means to augment the system performance. As stated by ITRS, 90% of the processor's chip area is occupied by SRAM [1]. For system-on-chips (SoCs) to achieve high density of integration, the size of CMOS transistors used in SRAM cell need to be down-scaled to nanometer regime. The width to length ratio of the MOS transistors used should be minimal. But this downscaling causes variations in parameters (e.g. threshold voltage V_t) of the transistors. These variations have an adverse impact on the read/write stability and reliability of the SRAM cell [2]. Due to high threshold voltage fluctuations, the conventional (CON6T) SRAM cell suffers failures in its functionality.

Various designs of SRAM cell using 6 to 10 transistors have been proposed by researchers. Mizuno *et al.* proposed a 6T SRAM cell which improved the access delay by 50% and reduced power consumption by 10% [3]. These improvements were observed at the cost of poor noise margin. Moreover, the use of negative voltage at the time of read operation adversely affected stability of the SRAM cell. Takeda *et al.* proposed a 7T-SRAM cell which operates at low supply voltage (V_{DD}) and provides high performance. But this cell had the problem of dynamic retention. Also, write margin decreased at a lower voltage and read operation was not reliable as it could destroy the data stored in the cell [4]. Another 7T SRAM cell proposed in [5] achieves higher read margin by cutting the pull down path to ground during read operation. But suffers from poor write-ability due to single ended write scheme. Chang *et al.* proposed a low-voltage, variability-tolerant, high-speed 8T-SRAM cell but the use of 8 transistors consumes larger area [6]. Authors in [7] used full transmission gate instead of pass transistor access gate to mitigate impact of process, voltage and temperature variations on design metrics of SRAM cell at the expense of read delay and write trip current. A. Islam *et al*. proposed a low leakage 10T SRAM cell which attains narrower spread in all design metrics at the expense of larger area overhead compared to conventional 6T SRAM cell [8]. Authors in [9] proposed 11T SRAM cell, which achieves improvement in leakage power at the expense of 84% area overhead compared to 6T SRAM cell. A 13T SRAM cell is proposed by authors in [10] that achieves lower write power dissipation due to reduction in switching activity. But it shows degradation of 49.5% in write static noise margin and also exhibits 76% higher read access time. In addition to that, it also occupies higher area as compared to conventional 6T SRAM cell.

Thus, in order to meet the density requirements of SRAM cell along with high performance and reliability, a proper trade-off between different design metrics of SRAM cell and device area must be maintained. This paper makes the following contributions in this direction:

1) This paper proposes a stable read decoupled 6T SRAM cell (hereafter called SRD6T), which performs single-ended read operation. The design metrics of the proposed SRD6T SRAM cell are compared to those of (CON6T) cell.
2) A single-ended read decoupled scheme is used to achieve higher RSNM by eliminating the chances of read disturb.

To verify our results, we employed extensive Monte Carlo simulations in SPICE using the 16-nm Predictive Technology Model (PTM) developed by the National Integration and Modeling (NIMO) Group at Arizona State University [11].

The remaining portion of the paper has been organized as follows. Section II provides device sizing and a discussion on the proposed SRD6T SRAM cell. The results of simulation and their comparison are presented in Section III. Finally, Section IV concludes the paper.

II. PROPOSED WORK AND DEVICE SIZING

In this paper, the proposed SRD6T is simulated for an SRAM cell array comprising of 256 cells in a row and 128 cells in a column. As shown in Fig. 1, the CON6T SRAM cell uses two pass access transistors, and thus, has two ports. The proposed SRD6T cell design as shown in Fig. 2, has a single port (to perform the read operation). Proposed cell design uses

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majority of PMOS transistors to earn the benefit of its higher tolerance towards radiation. Leakage current remains unaffected from radiation bombardment in PMOS transistor, but leakage current in NMOS transistor gets increased [12]. In addition, PMOS transistor exhibits very low flicker (1/f) noise compared to NMOS transistor. Moreover, the compressive stress offered by STI (shallow trench isolation) results in mobility degradation of electrons of NMOS rather than holes of PMOS near the edges of active region.

The CON6T cell has two ports and a voltage divider network is setup by the transistors MN3 (MN4) and MN1 (MN2). The read current flows from the bitlines to GND via this path. In the proposed design, the read operation is single ended and the read current flows from BL to GND through a separate read assist transistor MP3 and read access transistor MN3. MN3 is common for all the 256 cells in a row. The read current in this case does not flow through the pull-down driver NMOSFETs (MN1/MN2). This read-decoupled scheme employed during read operation drastically improves the read static noise margin (RSNM) as compared to CON6T. Also, the proposed cell uses a write assist transistor MP4 which is turned ON only during write operation.

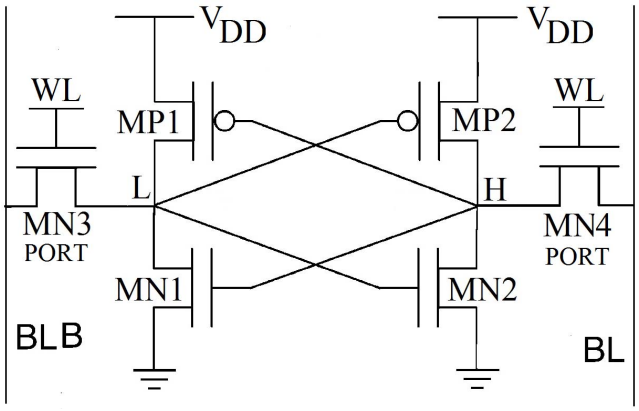

Fig. 1 Conventional 6T SRAM Cell.

In CON6T cell, read stability and write-ability are two conflicting design metrics. Therefore, improvement in read stability adversely affects the write-ability and vice-versa. But in the proposed cell design, the read operation takes place independently because of the read-decoupled scheme.

The channel length of all transistors used in the proposed cell and the CON6T cell are sized at the minimum value of 16 nm. Transition frequency f_T for short-channel devices is inversely proportional to channel length (L) [13]. Therefore, the use of minimum sized (i.e. channel length) devices is a critical piece of our design strategy. In the proposed design, channel width of all the PMOSFETs MP1, MP2, MP3 and MP4 are maintained at a minimum value of 16 nm. The channel width of all the pull-down driver NMOSFETs MN1 and MN2 are taken as 32 nm. Since, MN3 sinks the current from all the cells in the row, its channel width is taken as 64 nm. This helps in reducing read delay. The impact of 10% variation in supply voltage is analyzed by scaling down V_{DD} from 770 mV to 630 mV.

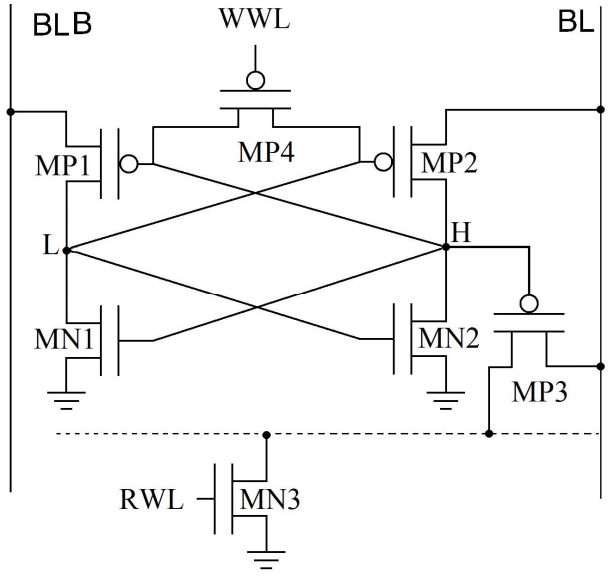

Fig. 2 Proposed SRD6T SRAM Cell.

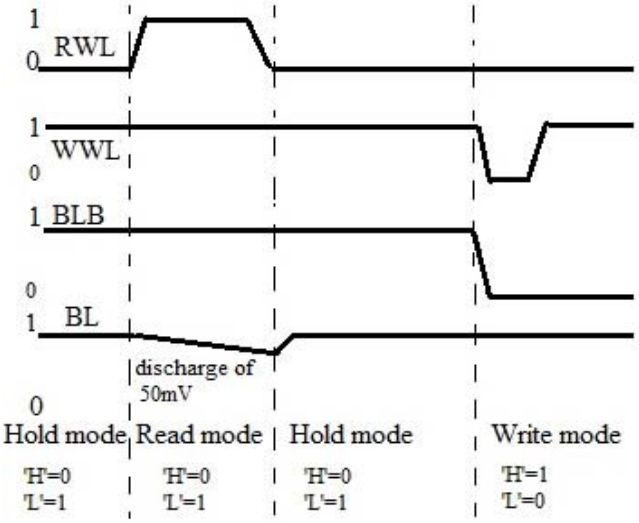

Fig. 3 BL, BLB, WWL and RWL status during read, write and hold modes.

III. Simulation Results and Discussions

In this section, the simulation results of read static noise margin (RSNM) and write static noise margin (WSNM) are discussed.

A. Read Static Noise Margin Analysis

Since Seevinck's seminal work in 1987, read stability has been quantified with the read static noise margin (RSNM), which is defined as the minimum amount of noise needed to upset the state of the cell [14]. RSNM is a measure of the stability during the cell's read operation. Its estimation is done by simulating the cell in its read mode i.e. keeping RWL and WWL high. RSNM is estimated graphically from the read voltage transfer curves (VTCs). The butterfly plot is thus obtained as shown in Fig. 4.

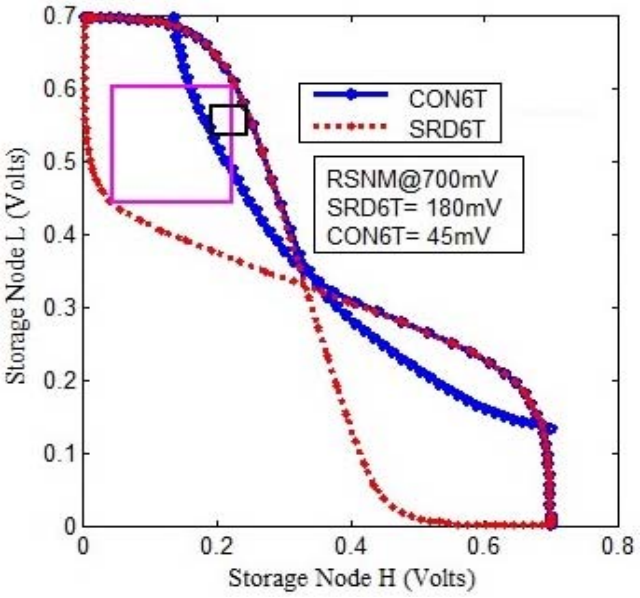

Fig. 4 Static voltage characteristics of SRAM cell during read operation.

RSNM is estimated as the length of the side of the largest-sized square that can be fitted into the butterfly curve's smaller lobe [15]-[16]. The plot in Fig. 4 shows that the proposed SRD6T cell achieves an RSNM of 180 mV whereas the CON6T cell exhibits and RSNM of 45 mV @ 700 mV. Hence, there is an improvement by a factor of 4. Figs. 5 and 6 show the read VTCs formed by butterfly curves from statistical method such as large number of Monte Carlo simulations of

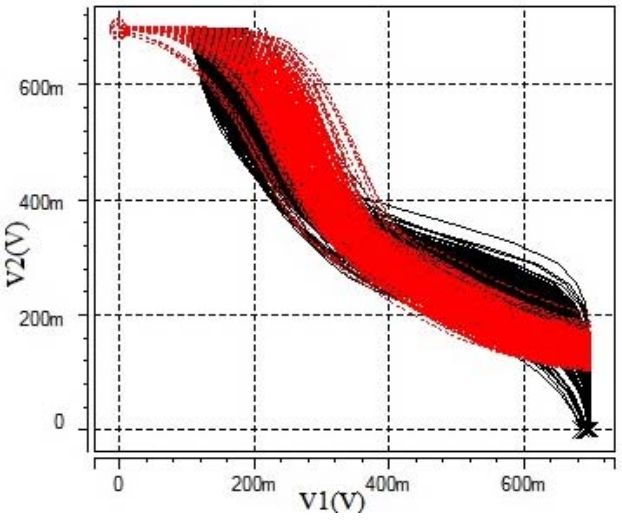

Fig. 5 Static voltage characteristics during read operation obtained from statistical method such as large number of Monte Carlo Simulations for CON6T SRAM cell

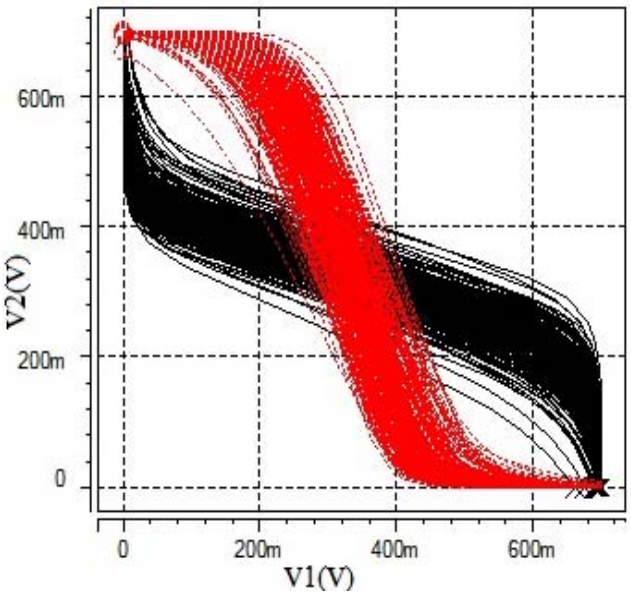

Fig. 6 Static voltage characteristics during read operation obtained from statistical method such as large number of Monte Carlo Simulations for proposed SRD6T SRAM cell.

SRD6T and CON6T circuits. Unlike the CON6T cell, the read current in the proposed design does not take the path via storage node and this eliminates the probability of read upset due to the voltage bump of the voltage divider network. This is the reason for the high improvement observed in RSNM.

B. Write Static Noise Margin Analysis(WSNM)

During write operation, the voltage at which logic '0' is to be written (suppose initially storing logic '1') has to be pulled down to a value low enough so as to flip the cell contents. This causes a '1' to be written at the other node. The ability of an SRAM cell to pull down this voltage is referred to as WSNM. Graphically, it is calculated as the length of the side of the smallest-sized square that can be fitted into the lower half of the read and write VTCs.

A successful write is ensured by the convergence of the read and write VTCs at the same point [15]-[16]. This can be verified from Fig. 7. The plot also shows that WSNM for the proposed design is 270 mV and for CON6T, it is 250 mV @ 700 mV. Thus, the proposed cell also shows improvement in WSNM by a factor of 1.08 (8%). Figs. 8 and 9 show static voltage characteristics during write operation obtained from statistical method such as large number of Monte Carlo simulations of CON6T and SRD6T SRAM cells.

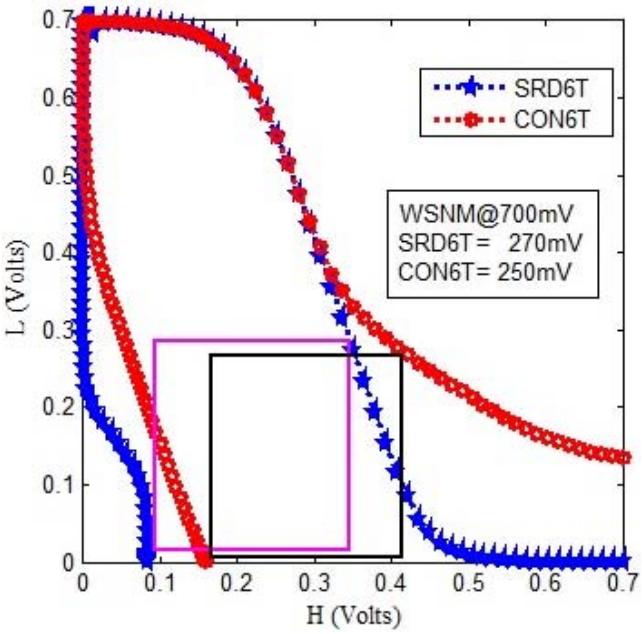

Fig. 7 Static voltage characteristics of SRAM cell during write operation.

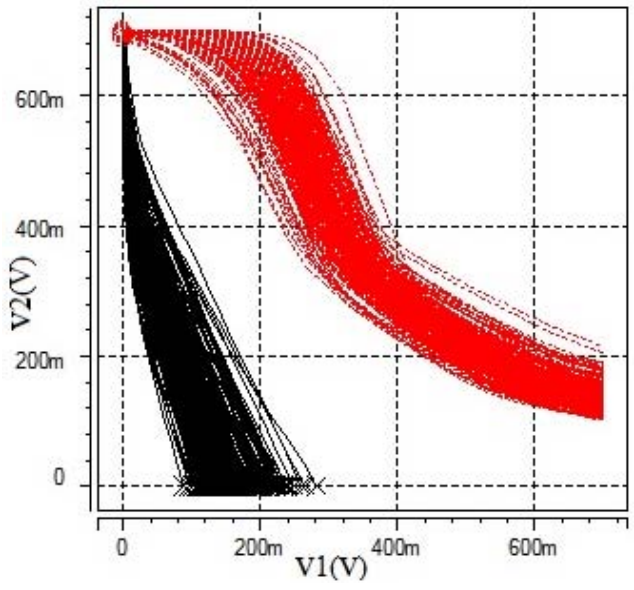

Fig. 8 Static voltage characteristics during write operation obtained from statistical method such as large number of Monte Carlo Simulations for CON6T SRAM cell.

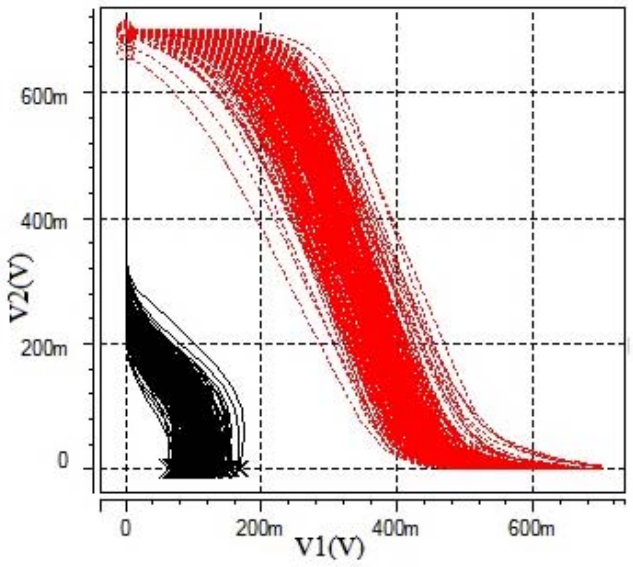

Fig. 9 Static voltage characteristics during write operation obtained from statistical method such as large number of Monte Carlo Simulations for proposed SRD6T SRAM cell.

IV. CONCLUSION

In this work, we have focused on improving the stability of an SRAM cell. We achieved this by proposing a novel SRD6T SRAM cell design which shows significant improvement in read SNM and marginal improvement in write SNM. The proposed cell's enhanced read stability and write ability are verified by extensive SPICE simulations. Thus, the SRD6T cell is a viable option where stability of the device is a major concern.

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