A Review of Low-Power Static Random Access Memory (SRAM) Designs

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***Abstract*— The growing demand for low-power static random access memory (SRAM) cells in Internet of Things (IoT) devices has led to the development of various SRAM cell topologies that minimize power consumption while maintaining performance and stability. In this paper, we have analyzed various SRAM designs based on different parameters, such as power dissipation, delay, area, energy, and stability. It is observed that 6T SRAM cell, consisting of six transistors, is the most widely used topology due to its simplicity and low area requirements. However, larger cells such as 8T, 9T, and 10T have been developed to improve stability and reduce power consumption, although they require more area. It has been observed8T work better for read delay while 9T works better for 9 Scaling down SRAM cells to smaller feature sizes presents challenges in maintaining stability and reliability while minimizing power consumption.**

Keywords*— *Static Random Access Memory (SRAM), Stability, Energy, Power Dissipation

I. INTRODUCTION

There is a trend towards using high-performance integrated circuits made with deep sub-micron technology. A lot of research has been done to develop portable devices for various emerging applications [1,2].SRAM is a type of computer memory that is widely used in various computing systems, such as CPUs, GPUs, and SoCs. Compared to other types of memory, such as DRAM, SRAM offers faster access times, lower latency, and higher data transfer rates [3]. SRAM stores data using a network of transistors, which form a latch or flip-flop that can hold one bit of data. The latch is composed of two cross-coupled inverters, and the state of the latch is maintained as long as power is supplied to the circuit. SRAM has the advantage of being able to retain data without the need for periodic refresh cycles, unlike DRAM which requires a periodic refresh to maintain data integrity [4].

There are several topologies for SRAM design, including the 6T, 7T, 8T, 9T, and 10T cells, each with its own advantages and disadvantages. The 6T cell is the most commonly used topology and consists of six transistors that form two cross-coupled inverters and two access transistors. The 7T cell adds a shared read/write data bus to the 6T cell, allowing for simultaneous read and write operations, and the 8T cell includes an error correction code (ECC) for improved data integrity. The 9T cell adds redundancy and selective refresh to the 6T cell, while the 10T cell includes both redundancy and selective write/read assist circuits for improved performance and data integrity [5].SRAM design is a complex process that requires careful consideration of several design parameters, including power dissipation, delay, area, energy, and stability. Different design techniques can be employed to optimize these parameters, such as voltage scaling, assist circuits, adaptive write timing control, and selective write and read operations. Additionally, as SRAM cells are integrated into larger memory arrays, issues such as leakage current, noise, and process variation become increasingly important to consider [6].

Overall, SRAM design plays a critical role in the performance and reliability of computing systems, and continued research and innovation in this area is necessary to meet the increasing demands of modern computing applications.

II. RELATED WORKS OF SRAM DESIGN

In this section, we have included the related work of various SRAM designs with its advantageous effects.

In [7] authors provides a comprehensive review of techniques for reducing leakage current in SRAMs. These techniques include circuit-level approaches, such as supply voltage scaling and data retention control, transistor-level approaches, such as gate oxide thickness scaling and threshold voltage adjustment, and system-level approaches, such as power gating and body-biasing.

In [8] authors presents a high-speed, low-power SRAM design that uses a dual-ported data-access scheme to reduce access time and power consumption. The proposed design also incorporates voltage boosting techniques to further improve performance and power efficiency.

In [9] authors present a 10T SRAM cell design that offers high stability and low leakage for high-performance applications. The proposed design uses a dual-threshold voltage technique to improve stability and a read-disturb-free scheme to reduce leakage current.

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In [10] authorspresents a 9T SRAM cell design that offers improved stability and reduced leakage power compared to traditional 6T SRAM cells. The proposed design uses a split read path and a body-biasing technique to achieve these improvements.

Compared to conventional 6T SRAM cells, the 8T SRAM cell design presented in [11] offers increased read and write stability. The proposed design uses a differential read scheme and a feedback-controlled write driver to achieve these improvements.

In [12] authors present a design and analysis of 12T SRAM cells that offer high stability and low power consumption. The proposed design uses a dual-Vth technique and a dynamic voltage scaling scheme to achieve these objectives.

In [13] authors present a high-speed, low-power, and ultra-low voltage SRAM design for the Internet of Things (IoT) applications. The proposed design uses a body-biasing technique and a dynamic voltage and frequency scaling scheme to achieve these objectives.

The authors present a dynamic voltage and frequency scaling technique for SRAMs in [14] to improve power consumption while preserving performance. The proposed technique uses a closed-loop control scheme to adjust the supply voltage and frequency based on workload and temperature.

In [15] authors present a dual-supply SRAM design that offers improved stability and reduced leakage power compared to traditional single-supply SRAMs. The proposed design uses a voltage-level shifting scheme and a word line-voltage control technique to achieve these objectives.

In [16] authors presents a fault-tolerant SRAM design for high-reliability applications, including radiation-hardened and automotive electronics. The proposed design uses a redundancy scheme and an error correction.

In [17] the paper presents a new design for a static random-access memory (SRAM) cell using a 7-transistor (7T) architecture that is optimized for sub-20 nm FinFET technologies. The proposed design addresses the challenges associated with sub-threshold voltage operation, which is necessary for low-power consumption, but can lead to reduced read and write margins. The authors demonstrate that their 7T SRAM cell achieves high write and read margins, as well as low write time, compared to other existing designs. They also show that their design is robust to process variations and temperature fluctuations. The paper provides detailed analysis and simulations to support the proposed design and its advantages. The results of this research could be useful for developing low-power, high-performance memory circuits for future integrated circuits.

In [18] paper presents a new 8-transistor SRAM cell design that is optimized for ultralow power applications. The proposed design uses differential sensing to improve the cell's robustness to process variations and reduce power consumption. The authors demonstrate through simulations that the proposed design achieves a 30% reduction in power consumption compared to a conventional 6T SRAM cell, while also maintaining similar read and write access times.

In [19] paper presents a new 9-transistor SRAM cell design that improves on the conventional 6T SRAM cell design by providing better read stability and write-ability. The authors use simulations to demonstrate that the proposed design achieves improved stability margins and reduced sensitivity to process variations. Additionally, the authors show that the proposed 9T SRAM cell has a higher write margin and lower write power consumption compared to the conventional 6T SRAM cell.

In [20] paper presents a new 10-transistor (10T) SRAM cell design that is optimized for low-leakage and subthreshold operation. The proposed design uses a positive feedback technique called the "positive pulse generation network" (PPN) to improve read stability and reduce write disturbance. The authors demonstrate through simulations that the proposed design achieves a 2.6x reduction in standby leakage current compared to a conventional 6T SRAM cell, while also maintaining similar read and write access times. Additionally, the proposed design is shown to be more resilient to process variations and supply voltage fluctuations than a conventional 6T SRAM cell, making it a promising option for low-power applications.

In [21] paper proposes a low-swing transmitter network for multi-bank SRAM arrays that reduces both power consumption and signal integrity issues. The proposed design is shown to achieve up to 48% power reduction and up to 64% signal amplitude improvement compared to previous designs.

In [22] paper proposes a new 7T SRAM cell with a dual-port configuration that enables simultaneous read and write operations with reduced power consumption and improved performance. The read/write assist circuit is used in the proposed design to increase the stability of the cell during read and write operations while also reducing the space and consumption of power on the cell. The suggested 7T SRAM cell surpasses the current 6T and 8T SRAM cells in terms of write margin, power usage and read access time the authors show.

In [23] paper presents a low power and high reliability 9T SRAM design with selective write-word line-assist (SWWA) that selectively enhances the write operation of the memory cell. The SWWA technique uses an auxiliary write word line and an additional write driver to apply a higher voltage to the memory cell during ximproving the write margin of the cell. Detailed simulations are used to assess the proposed 9T SRAM cell and compare it to the 6T and 8T SRAM cells now in use. The findings demonstrate that the proposed 9T SRAM cell delivers considerable reductions in power consumption, write margin, and write access time.

In [24] authors compare a new 8-transistor SRAM cell to traditional standard cells (6T, 8T, 9T, and 10T) and focus on improving the reading operations. The proposed SRAM cell aims to separate the read and write operations, which eliminates the need for bit line pre-charging and simplifies the simultaneous read and write operations. The study found that the new SRAM cell reduces the read delay for read 0 by 80.70% to 83.70% and read 1 latency by 88.16% to 90%, compared to the traditional cells. Additionally, the new SRAM cell provides enhanced noise margins and lower power consumption, but the study highlights the need for improvement in power consumption and asymmetric operation in future work.

This [25] paper describes a new type of SRAM bit cell with 7 transistors, which is compared to its pre- existing counterparts with 6, 7, 8, 9, and 10 transistors. The proposed 7T cell has a single bit-line architecture that reduces its switching activity factor and is designed for a 32 nm feature size at a 300 mV supply voltage. The study found that the

proposed 7T cell has several advantages over its counterparts, including a better static performance for hold operation and write margin, faster write operation, and reliable performance under PVT variations, all achieved with minimal power consumption. The proposed 7T cell has a smaller area footprint than most of its counterparts, except for the 6T cell, which has a slightly smaller area. The study concludes that the proposed 7T cell is a viable alternative to other bit cells.

III. SRAM TOPOLOGIES

SRAMs have various topologies, each with its own advantages and disadvantages. The performance comparison of several SRAM topologies will be covered in this section.

A. 6T SRAM

The 6T SRAM is the most widely used SRAM topology. It consists of six transistors, which are organized into two cross-coupled inverters and two access transistors. The 6T SRAM is simple and small in size, making it ideal for high-density memory applications. However, it has a relatively high leakage current, which can result in power consumption and reliability issues.

B. 7T SRAM

A further transistor acts as a switch to detach one of the two inverters from the bit line in the 7T SRAM, which is a modified version of the 6T SRAM.This extra transistor provides a way to reduce the read disturbance caused by the half-selected word lines, which can affect the stability of the stored data. The 7T SRAM is also less sensitive to process variations than the 6T SRAM, which improves its yield and reliability. However, the 7T SRAM has a larger area and higher power consumption than the 6T SRAM.

C. 8T SRAM

The 8T SRAM is an enhanced version of the 6T SRAM, with two additional transistors that separate the storage node from the access transistors. This separation reduces the leakage current and improves the stability of the stored data. However, the extra transistors increase the size and complexity of the 8T SRAM, making it less suitable for high-density memory applications.

D. 9T RAM

Another enhanced variation of the 6T SRAM is the 9T SRAM, which adds an additional transistor between the storage node and the ground. Similar to the 8T SRAM, this extra transistor offers a means of lowering the leakage current and enhancing data stability. Nonetheless, the 9T SRAM can be employed in high-density memory applications despite having a smaller size than the 8T SRAM. Due to the additional transistors in the access path, the 9T SRAM has a slower access time than the 6T and 8T SRAM.

E. 10T SRAM

The 10T SRAM is another improved version of the 6T SRAM, with two additional transistors that enable read and write operations while preventing data corruption due to process variations. The 10T SRAM has lower leakage current and better noise immunity compared to the 6T SRAM. However, it has a larger area and slower access times.

In conclusion, each SRAM topology has its own advantages and disadvantages, and the topology chosen relies on the particular application's needs. The 6T SRAM is the most commonly used topology, while the other topologies are used for specialized applications that require specific performance characteristics such as reduced leakage current, multi-port access, or higher stability.

TABLE I. SRAM TOPOLOGIES COMPARISION

SRAM Topologies Comparisons		
SRAM Topology	**Advantages**	**Disadvantages**
6T SRAM	Small size, simple design	High leakage current, lower data stability
7T SRAM	Reduced read disturbance, improved yield and reliability	Larger area, higher power consumption
8T SRAM	Reduced leakage current, improved data stability	Larger size, more complex circuitry
9T SRAM	Smaller area than 8T, reduced leakage current, improved data stability	Slower access times than 6T and 8T
10T SRAM	Lower leakage current, better noise immunity	Larger area, slower access times

IV. COMPARATIVE ANALYSIS BASED ON DESIGN PARAMETERS

A comparative analysis of different SRAM cell's performance based on various design parameters:

Power Dissipation: The power dissipation of an SRAM cell is an important parameter to consider, especially for battery-powered devices. Here's how different SRAM cells compare in terms of power dissipation:

- 6T SRAM has the lowest power dissipation due to its small size and simple design.
- 8T and 10T SRAM cells have higher power dissipation than the 6T SRAM due to their larger size and additional transistors.
- 7T and 9T SRAM cells have even higher power dissipation than 8T and 10T SRAM due to their larger size and extra access transistor.

Delay: The delay of an SRAM cell determines how quickly data can be read or written. Here's how different SRAM cells compare in terms of delay:

- 8T and 10T SRAM cells have the lowest delay due to their reduced leakage current and improved data stability.
- 6T SRAM has a moderate delay due to its simple design and lower data stability.
- 7T and 9T SRAM cells have a higher delay due to their larger size and extra access transistor.

Area: The area of an SRAM cell is an important factor in determining the overall size and cost of a memory system. Here's how different SRAM cells compare in terms of area:

- 6T SRAM has the smallest area due to its simple design and fewer transistors.
- 7T and 9T SRAM cells have a larger area than the 6T SRAM due to their extra access transistor.
- 8T and 10T SRAM cells have the largest area due to their additional transistors.

Energy: The energy consumption of an SRAM cell is a key factor in determining the overall power consumption of a memory system. Here's how different SRAM cells compare in terms of energy:

- 6T SRAM has the lowest energy consumption due to its simple design and smaller size.
- 8T and 10T SRAM cells have higher energy consumption than the 6T SRAM due to their larger size and additional transistors.
- 7T and 9T SRAM cells have even higher energy consumption than 8T and 10T SRAM due to their larger size and extra access transistor.

Stability: The stability of an SRAM cell determines how well it retains the stored data over time. Here's how different SRAM cells compare in terms of stability:

- 8T and 10T SRAM cells have the highest stability due to their reduced leakage current and improved data stability.
- 6T SRAM has moderate stability due to its simple design and lower data stability.
- 7T and 9T SRAM cells have lower stability than 8T and 10T SRAM due to their larger size and extra access transistor.

The choice of an SRAM cell topology depends on the specific trade-offs between these designs parameters that are required for a particular application. The 8T and 10T SRAM cells offer better performance in terms of delay, energy, and stability, but at the cost of larger size and higher power dissipation. The 6T SRAM cell offers a smaller size and lower power dissipation, but at the cost of lower data stability and longer access times. The 7T and 9T SRAM cells offer some advantages over the 6T SRAM without incurring the size penalty of the 8T and 10T SRAM cells, but have higher power consumption and access delay.

However, it is shown from the referred paper that the 8T SRAM cell has the best read performance among the SRAM cells compared in the table, while the 9T SRAM cell has the best write performance. The 7T SRAM cell has the lowest read and write power consumption, while the 10T SRAM cell has the highest write power consumption. Overall, each SRAM cell has its own advantages and trade-offs in terms of various parameters such as power consumption, delay, and stability. The choice of which SRAM cell to use depends on the specific requirements and constraints of the application.

TABLE II. TABLE TYPE STYLES

Parameters	***Conv. 6T SRAM***	***7T SRAM [17]***	***8T SRAM [18]***	***9T SRAM [19]***	***10T SRAM [20]***
Vdd (V)	1.0	1.0	1.0	1.0	1.0
WSNM (mV)	365	440	355	390	345
Read power (μW)	6.18	6.77	4.65	4.74	6.18
Leakage power (MC) (pW)	18.61	6.21	26.55	25.87	25.05
Write power (nW)	178	14.93	138.2	257.5	312.5
Read energy (aJ)	211.1	181.48	89.29	105.01	127.23
Read access time (pS)	67.23	52.15	36.90	40.86	40.52
Write energy (aJ)	13.56	1.28	8.41	13.80	59.09
Write access time (pS)	75.79	89.24	62.62	53.60	189.1

V. CONCLUSION

In this paper, we have observed various design models for SRAM and the design parameters for SRAM. We have also compared the different SRAM designs 6T, 7T, 8T, 9T, and 10T based on various parameters such as power dissipation, delay, area, energy, and stability. The choice of SRAM design among 6T, 7T, 8T, 9T, and 10T depends on the specific application requirements.

For applications that require faster read/write times and lower power consumption, 6T and 7T cells may be preferred, while applications that prioritize stability and larger cell size may favor 8T, 9T, and 10T cells. For applications that prioritize speed and low power consumption, the 6T and 7T cells may be preferred. On the other hand, applications that require higher stability or larger cell sizes may benefit from larger cells like 8T, 9T, and 10T. The choice may also depend on other factors like cost, availability of fabrication technology, and tradeoffs between different design parameters.

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