Printed Pages : 7 **MCA – 215**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 7307 Roll No. | | | | | | | | | | |

M. C. A.

(SEM. II) EXAMINATION, 2008-09

COMPUTER ORGANIZATION

Time : 3 Hours] *[Total Marks : 100*

Note : This paper is in **three** sections. Section A carries **20** marks, Section B carries **30** marks and Section C carries **50** marks.

SECTION–A

1 You are required to answer all the parts : **2×10=20**

Choose correct answer for the following parts :

(a) Exponent in floating point number representation is biased to :

(i) enhance the range of representation

(ii) avoid comparing sign bits of exponent in floating point arithmetic operation.

(iii) to facilitate representation of zeros

(iv) both (ii) and (iii) are true.

(b) A stack pointer register is always associated with a :

(i) hardwired stack

(ii) Software stack to indicate top of the stack element

(iii) Hardware stack to store stack capacity

(iv) None of the above is true.

(c) The implied one-bit to the left of fractional mantina of IEEE 754 floating point format is used to facilitate.

(i) enhancement of precision

(ii) representation of NaN (not a number) representation

(iii) enhancement of the range of representation;

(iv) representation of sign bit.

(d) Program size is likely to be minimum with :

(i) Expanding opcode

(ii) fixed length opcode

(iii) data dependent opcode

(iv) None of the statements is valid.

(e) A microprogram sequencer :

(i) enables efficient handling of microprogram subroutines.

(ii) help appropriate encoding and decoding of control signals in control memory.

(iii) control the generation of effective address for the control ROM.

(iv) handles the task of next address generation in a microprogrammed control structure.

(f) A typical vertical microinstruction format is characterized by :

(i) limited encoding with limited parallilism

(ii) limited encoding with high degree of parallilism

(iii) high degree of encoding with high degree of parallilism

(iv) high degree of encoding with limited parallilism.

(g) A CPU handles interrupt by executing interrupt service routine.

(i) whenever an interrupt is registered

(ii) by checking interrupt register after execution of each instruction.

(iii) by checking interrupt register at the end of fetch cycle.

(iv) by checking interrupt register at regular times interval.

(h) The CPU state is saved in the event of a transfer control.

(i) from one instruction to a non-sequential instruction of a program

(ii) from our program to another

(iii) during execution of an instruction due to an interrupt cycle.

(iv) None of the above statement is true.

(i) An instruction with an indexed operand having address field with all O's bit is effectively a'.

(i) register direct mode of operation

(ii) register indirect mode of operation

(iii) memory indirect mode of operation

(iv) base register addressing mode of operation.

(j) The delay element method of controller design employs:

(i) encoded control states

(ii) modulo-K counter to control K repetitive actions.

(iii) Control structure directly reflecting the behaviour

(iv) None of the above is valid.

SECTION–B

2 Answer any **three** parts of the following : **10×3=30**

(a) (i) Show the block diagram of the hardware that implements the following register transfer statement

$T : R2 \leftarrow R1, R1 \leftarrow R2$

(ii) Describe the design of 4-bit carrylook ahead adder.

(b) Write short notes on microprogram sequencing and microinstruction with next address field.